

APPLICATION
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TITLE: LOW-LOSS TRANSFORMER-COUPLED GATE DRIVER

APPLICANT: PATRIZIO VINCIARELLI

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LOW-LOSS TRANSFORMER-COUPLED GATE DRIVER

TECHNICAL FIELD

This application is a division of pending U.S. application Serial No. 10/443,573, filed May 22, 2003 (incorporated herein by reference) which is a continuation-in-part of pending U.S. application Serial No. 10/264,327, filed October 1, 2002 (incorporated herein by reference) which is a continuation-in-part of U.S. application Serial No. 10/066,418, filed January 31, 2002 (now abandoned).

This invention relates to the field of electrical power conversion and more particularly to distributed electronic power conversion systems.

BACKGROUND

DC-DC converters transfer power from a DC electrical input source to a load by transferring buckets of energy between windings of an isolation transformer. The DC output voltage delivered to the load is controlled by adjusting the timing of internal power switching elements (*e.g.*, by controlling the converter switching frequency and/or the switch duty cycle and/or the phase of switches). As defined herein, the functions of a "DC-DC converter" comprise: a) isolation between the input source and the load; b) conversion of an input voltage to an output voltage; and c) regulation of the output voltage. DC-DC converters may be viewed as a subset of a broad class of switching power converters, referred to as "switching regulators," which convert power from an input source to a load by processing energy through intermediate storage in reactive elements. As defined herein, the functions of a "Switching Regulator" comprise: a) conversion of an input voltage to an output voltage, and b) regulation of the output voltage. If the required output voltage is essentially a positive or negative integer (or rational) multiple of the input voltage, the conversion function may also be efficiently performed by a capacitive "Charge Pump," which transfers energy by adding and subtracting charge from capacitors.

The introduction of commercial DC-DC converters capable of efficiently switching at high frequencies (*e.g.*, 1 MHz) has brought about significant miniaturization of the DC-DC converter function. The reduction in switching losses made possible by the invention, in the early 1980's, of zero current switching ("ZCS") and zero voltage switching ("ZVS") power

conversion topologies, led to an increase in converter operating frequency that translated into a commensurate breakthrough in power density. The power density of DC-DC converters jumped from about 1 Watt/cubic inch to over 20 Watts/cubic inch. The reduction of DC-DC converter volume per unit of power delivered, and the corresponding reduction in DC-DC converter weight, created many new opportunities for the deployment of DC-DC converters and enabled the development of more advanced power systems and power system architectures for electronic products and systems. These products and systems have also benefited from advances in power density and efficiency of commercial Switching Regulators and Charge Pumps.

High frequency DC-DC converters have been packaged to provide flexibility in mechanical mounting and thermal management. A typical DC-DC converter (Fig. 1) is an enclosed assembly comprising a metal surface for extracting heat and connection pins for connecting the converter to the source and the load. Contemporary DC-DC converters, commercially available from many vendors, offer power densities up to 100 Watts per cubic inch and the height of the overall assembly, exclusive of the pins, is typically 0.5 inch.

It is known that there is a tradeoff between DC-DC converter operating efficiency and power density on the one hand, and the range of input voltages over which the converter is designed to operate on the other. Narrower input voltage operating ranges may allow for more efficient converters and higher power densities. It is also known that, for a given level of power delivery, the efficiency of a power converter typically decreases with decreasing output voltage. For example, a converter delivering 2V at 100 Amperes (100 Watts) will typically exhibit higher losses than a converter delivering 5V at 20 Amperes (100 Watts).

Certain electronic systems contain a multiplicity of subsystems on printed circuit boards ("PCBs"), closely spaced and interconnected within an enclosure or rack, each PCB requiring a complement of voltages suitably adapted to the unique power requirements of the circuitry on the PCB. Prior to the availability of high density and low profile (0.5 inch tall) DC-DC converters, most such systems relied on a "centralized power architecture" ("CPA"). In the CPA architecture, the various well-regulated voltages required by the PCBs (e.g., 2V, 5V, 12V) are generated in a centralized power supply and bussed around the system for delivery to each of the PCB subassemblies. With the CPA architecture, high currents at relatively low voltages need to be delivered over substantial distances and the management of power losses and voltage drops throughout the system is difficult and costly. The advent of high-density DC-DC converters

enabled a migration from the CPA to a “distributed power architecture” (“DPA”). In the DPA architecture, these problems are overcome by bussing a relatively higher, less well-regulated, voltage around the system (*e.g.*, 300V, 48V, 24V) to provide input power to DC-DC converters on the PCBs, which perform the functions of isolation, voltage conversion and regulation at the point-of-load. In addition to simplifying power distribution, the DPA provides system design flexibility, since each subsystem can be provided with DC-DC converters which deliver whatever voltages are needed without requiring modifications to a centralized power supply or distribution system. System design flexibility is further enhanced by the availability of high density Switching Regulators and Charge Pumps.

The DPA architecture is discussed in Tabisz et al, “Present and Future of Distributed Power Systems,” APEC '92 Conference Proceedings, 1992, pp. 11 –18; in Mweene et al, A High-Efficiency 1.5 kW, 390-50V Half-Bridge Converter Operated at 100% Duty Ratio,” APEC '92 Conference Proceedings, 1992, pp. 723-730; in Choi et al, “Dynamics and Control of DC-to-DC Converters Driving Other Converters Downstream,” IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications, October 1999, pp. 1240-1248; and in Lee et al, “Topologies and Design Considerations for Distributed Power System Applications,” Proceedings of the IEEE, June 2001, pp. 939-950.

Non-resonant full-bridge, half-bridge, and push-pull DC-to-DC transformer topologies are known. *See e.g.*, Severns and Bloom, “Modern DC-to-DC Switchmode Power Conversion Circuits,” ISBN 0-442-21396-4, pp. 78 –111. Series, parallel, and other resonant forms of switching power converters are also known. *See e.g.*, Steigerwald, “A Comparison of Half-Bridge Resonant Converter Topologies,” IEEE Transactions on Power Electronics, Vol. 2, No. 2, April 1988. Variable frequency, series resonant, half-bridge converters for operation from an input voltage source are described in Baker, “High Frequency Power Conversion With FET-Controlled Resonant Charge Transfer,” PCI Proceedings, April 1983, and in Nerone, U.S. Patent 4,648,017. Half-bridge, single-stage, ZVS, multi-resonant, variable frequency converters, which operate from an input voltage source are shown in Tabisz et al, U.S. Patent No, 4,841,220 and Tabisz et al, U.S. Patent No, 4,860,184. A variable frequency, full-bridge, resonant converter, in which an inductor is interposed between the input source and the resonant converter is described in Divan, “Design Considerations for Very High Frequency Resonant Mode DC/DC Converters,” IEEE Transactions on Power Electronics, Vol. PE-2, No. 1, January, 1987. A

variable frequency, ZVS, half-bridge LLC series resonant converter is described in Bo Yang et al, "LLC Resonant Converter for Front End DC-DC Conversion," CPES Seminar 2001, Blacksburg, VA, April 2001. Analysis and simulation of a "Low Q" half-bridge series resonant converter, wherein the term "Low Q" refers to operation at light load, is described in Bo Yang et al, "Low Q Characteristic of Series Resonant Converter and Its Application," CPES Seminar 2001, Blacksburg, VA, April 2001.

Fixed-frequency half-bridge and full-bridge resonant converters are also known in which output voltage control is achieved by controlling the relative timing of switches. A half-bridge, single-stage, ZVS, multi-resonant, fixed-frequency converter that operates from an input voltage source is shown in Jovanovic et al, U.S. Patent No, 4,931,716. A full-bridge, single-stage, ZVS, resonant, fixed-frequency converter that operates from an input voltage source is shown in Henze et al, U.S. Patent No. 4,855,888.

A full-bridge, single-stage, ZCS, series-resonant, fixed-frequency converter, operating at a frequency equal to the characteristic resonant frequency of the converter, is shown in Palz, "Stromversorgung von Satelliten – Wanderfeldröhren hoher Leistung" ("Power Supply for Satellites - High Capacity Traveling-Wave Tubes"), Siemens Zeitschrift, Vol. 48, 1974, pp. 840-846. Half and full-bridge, single-stage, ZVS, resonant, converters, for powering fluorescent tubes are shown in Nalbant, U. S. Patent No. 5,615,093.

A DC-to-DC Transformer offered for sale by SynQor, Hudson, MA, USA, called a "BusQor™ Bus Converter," that converts a regulated 48VDC input to a 12 VDC output at a power level of 240 Watts and that can be paralleled with other similar converters for increased output power delivery, and that is packaged in a quarter brick format, is described in data sheet "Preliminary Tech Spec, Narrow Input, Isolated DC/DC Bus Converter," SynQor Document No. 005-2BQ512J, Rev. 7, August, 2002.

The art of resonant power conversion, including operation below or above resonant frequency, utilizing either ZCS or ZVS control techniques and allowing the resonant cycle to be either completed or purposely interrupted, is summarized in Chapter 19 of Erickson and Maksimovic, "Fundamentals of Power Electronics," 2nd Edition, Kluwer Academic Publishers, 2001.

Cascaded converters, in which a first converter is controlled to generate a voltage or current, which serves as the source of input power for a DC-to-DC transformer stage, are known.

A discussion of canonical forms of cascaded converters is given in Severns and Bloom, *ibid*, at, e.g., pp. 114-117, 136-139. Baker, *ibid*, discusses the use of a voltage pre-regulator cascaded with a half-bridge, resonant, variable-frequency converter. Jones, U.S. Patent No. 4,533,986 shows a continuous-mode PWM boost converter cascaded with both PWM converters and FM resonant half-bridge converters for improving holdup time and improving the power factor presented to an AC input source. A zero-voltage transition, current-fed, full-bridge PWM converter, comprising a PWM boost converter delivering a controlled current to a PWM, full-bridge converter, is shown in Hua et al, "Novel Zero-Voltage Transition PWM Converters," IEEE Transactions on Power Electronics, Vol. 9, No. 2, March, 1994, p. 605. Stuart, U.S. Patent No. 4,853,832, shows a full-bridge series-resonant converter cascaded with a series-resonant DC-to-DC transformer stage for providing AC bus power to distributed rectified loads. A half-bridge PWM DC-to-DC transformer stage for use in providing input power to point-of-load DC-DC converters in a DPA is described in Mweene et al, *ibid*. Schlecht, U.S. Patent Nos. 5,999,417 and 6,222,742 shows DC-DC converters which incorporate a DC-to-DC transformer stage cascaded with a switching regulator. Vinciarelli, "Buck-Boost DC-DC Switching Power Conversion," U.S. Patent Application No. 10/214,859, filed August 8, 2002, assigned to the same assignee as this application and incorporated by reference, discloses a new, high efficiency, ZVS buck-boost converter topology and shows a front-end converter comprising the disclosed topology cascaded with a DC-DC converter and a DC-to-DC transformer.

A power distribution architecture proposed by Intel Corporation, Santa Clara, CA, USA, called NPSA ("New Power Supply Architecture"), is described by Colson in "Intel Platform Solutions," Issue 23, September, 1999, and by Reynolds in "Intel Development Forum Highlights: Fall 1999," published by Gartner, Dataquest, November, 1999. NPSA comprises a front-end converter which generates a 30 VAC, 1 MHz, distribution bus for delivery to regulating AC-DC converters located near distributed loads. A power distribution architecture comprising a front-end converter which generates a 12 VDC distribution bus for use by point-of-load isolated and non-isolated converters is described briefly in "Tiny Titans: Choose 'Em and Use 'Em With Care," EDN magazine, May 2, 2002, p. 48. A power distribution architecture comprising a front-end isolated bus converter which generates an unregulated 12 VDC distribution bus for use by point-of-load non-isolated regulating DC-DC converters is described

in "Distributed Power Moves To Intermediate Voltage Bus," Electronic Design magazine, September 16, 2002, p. 55.

The accepted approach for delivering power to future generation microprocessors revolves around power conversion topologies and control techniques that support high-
5 bandwidth performance under closed-loop control. The strategy is to keep the voltage at the microprocessor within an allowable range under rapid transitions in the current drawn by the microprocessor by: a) providing adequate bypass capacitance at the point-of-load to absorb the rate of change of current within a time scale shorter than the response time of the upstream power converter and b) providing a converter having a very fast closed loop response to limit the
10 amount of point-of-load capacitance that is needed.

This approach relies upon the "multiphase buck topology" employing N buck converters operating in parallel, locked at the highest practical frequency and "interleaved" by a phase equal to $360/N$. Interleaving provides faster transient response by allowing a reduction in the value of the inductance in series with the output of each buck stage (thus increasing the slew rate of
15 current) and by allowing sampling of the output error voltage at N times the base frequency (thus extending the Nyquist limit for closed loop stability to a fraction of the multiplied frequency as opposed to the base frequency). As the microprocessor current and current rate of change keeps growing with every generation of microprocessor, more and more phases are added to keep up with it. And control methods to extract the most in terms of close loop bandwidth are being
20 developed.

An example of this microprocessor power paradigm (using double-edge modulation to extract closed-loop bandwidth in the 1.5 MHz range from a system consisting of 8 interleaved buck converters each operating at 1MHz) is discussed in "New Control Method Boosts Multiphase Bandwidth," Paul Harriman, Power Electronics, January 2003, pp. 36-45.

25 A series resonant converter in which ZVS is accomplished by exploiting the flow of magnetizing current in a transformer, or in an inductor connected in parallel with the primary winding of a transformer, is described in Ferreira, U. S. Patent No. 5,448,467.

Low-loss gate drivers for driving capacitive gate terminals of power switching devices are described in Yao et al, "A Novel Resonant Gate Driver for High Frequency Synchronous
30 Buck Converters," IEEE Transactions on Power Electronics, Vol. 17, No. 2, March 2002 and in

Fisher et al, U. S. Patent No. 5,179,512, in Steigerwald, U. S. Patent No. 5,514,921 and Schlecht, *ibid.*

A variety of isolated power conversion topologies are compared for use as voltage regulator modules ("VRM") in Ye et al, "Investigation of Topology Candidates for 48V VRM," 2002 APEC Conference. Projected trends in performance requirements for VRMs and a proposed technology roadmap for achieving those requirements are summarized in Stanford, "New Processors Will Require New Powering Technologies," Power Electronics Technology magazine, February 2002.

Modulating the channel resistance of a MOSFET synchronous rectifier switch as a means of regulating an output voltage of a switching power converter is described in Mullett et al, U. S. Patent No. 6,330,169 B2.

SUMMARY

In general, one aspect features an apparatus for driving a control input of one or more power switching devices. The apparatus includes a drive transformer having a secondary winding. A plurality of switches each of which have a control terminal referenced to a common signal reference for turning the switch ON and OFF and an output connected to drive the transformer. The plurality of switches include a first switch and a second switch being respectively poled to induce a magnetic flux in the drive transformer in a first and in a second direction when ON. The secondary winding is connected to drive the control inputs of the one or more power switching devices. A control circuit is connected to the control terminals and configured to operate the first and second switches in a series of control cycles. Each control cycle has two ON intervals during which one of the first and second switches is ON, and two OFF intervals during which both of the first and second switches is OFF and energy stored in the drive transformer is used to charge and discharge parasitic output capacitances of the plurality of switches and a parasitic input capacitance of the one or more power switching devices.

Implementations of the apparatus may include one or more of the following features. The power switching devices may include a pair of complementary switching devices which are OFF during a portion of the OFF interval. The pair of complementary switching devices is connected to drive a power transformer and a magnetizing inductance of the power transformer has a value small enough to allow ZVS of the complementary switching devices during the time

period when the complementary switching devices are OFF. The magnetizing inductance of the drive transformer has a value that allows ZVS of the first and second switches during the OFF intervals. The plurality of switches includes exactly two switches and the control terminals of the switches are referenced to ground. The transformer has a primary winding driven by the first and second switches, the first switch is connected as a primary switch, and the second switch is connected to the primary winding and a capacitor as a reset circuit. The transformer has a first and a second primary winding driven respectively by the first and second switches, and the control terminals of the first and second switches are referenced to ground. An inductive clamp circuit is connected across each of the primary windings, each clamp circuit has a clamp switch and a clamp diode, each clamp switch is turned ON during a portion of one of said OFF intervals, and each clamp circuit is poled to carry the magnetizing current flowing in its respective winding when its respective clamp switch is ON.

In general, another aspect features a method for driving a control input of one or more power switching devices. The method includes using a secondary winding of a drive transformer to drive the control inputs of the power switching devices, using a plurality of switches to drive the drive transformer, connecting a control terminal of each switch to reference a common signal reference for turning the switch ON and OFF, using a first switch and a second switch to respectively induce a magnetic flux in the drive transformer in a first and in a second direction when ON; and operating the first and second switches in a series of control cycles. Each control cycle includes two ON intervals during which one of the first and second switches is ON and two OFF intervals during which both of the first and second switches is OFF and energy stored in the drive transformer is used to charge and discharge parasitic output capacitances of the plurality of switches and a parasitic input capacitance of the one or more power switching devices.

Implementations of the method may include one or more of the following features. A pair of complementary switching devices may be used for the power switching devices and a sub-interval may be provided during a portion of the OFF interval when the pair of complementary switching devices is OFF. The pair of complementary switching devices may be connected to drive a power transformer and a value of magnetizing inductance may be provided in the power transformer to allow for ZVS of the complementary switching devices during the sub-interval. A value of magnetizing inductance may be provided in the drive transformer to allow for ZVS of the first and second switches during the OFF intervals. The plurality of

switches may have exactly two switches and the control terminals of the switches may be referenced to ground. The first switch may be used to drive a primary winding of the drive transformer as a primary switch and the second switch and a capacitor may be used as a reset circuit for the drive transformer. The first and second switches may be used to respectively drive a first and a second primary winding of the drive transformer and the control terminals of the first and second switches may be connected to reference ground. An inductive clamp circuit may be used across the primary windings to carry magnetizing current during a portion of one of the OFF intervals.

In general, another aspect features an apparatus for delivering a unipolar control voltage. The apparatus includes a transformer having a primary winding, a secondary winding, and a magnetizing inductance. Drive circuitry connected to drive the primary winding produces a bipolar voltage across the secondary winding. A first output terminal and a reference terminal deliver the control voltage. Switch circuitry connected to the secondary winding may be adapted to (a) connect the secondary winding across the first output terminal and the reference terminal when a voltage across the secondary winding is of a first polarity, (b) clamp the first output terminal to the reference terminal when a voltage across the secondary winding is of a second polarity, and (c) enable recycling of energy between the magnetizing inductance of the transformer and the parasitic capacitances of the switch circuitry and the capacitance between the first output terminal and the reference terminal.

Implementations of the apparatus may include one or more of the following features. The capacitance between the first output terminal and the reference terminal may be a parasitic gate-source capacitance of a MOSFET switch. The switch circuitry may include a MOSFET. A first controlled switch may have a first control input connected to the first output terminal. The switch circuitry may have a first switch connected between a first end of the secondary winding and the reference terminal and a second switch connected between a second end of the secondary winding and the reference terminal. The first output terminal may be connected to the second end of the secondary winding. A first controlled switch may have a first control input connected to the first output terminal, the first switch may have a control input connected to the second switch, the second switch may have a control input connected to the first switch, and the first and second switches may have a control threshold which is less than a control threshold of the controlled switch. A second output terminal may be connected to the first end of the secondary

winding for delivering a second unipolar control voltage relative to the reference. A second controlled switch may have a second control input connected to the second output terminal. The switch circuitry may be further adapted to: (d) connect the secondary winding across the second output terminal and the reference terminal when a voltage across the secondary winding is of the second polarity; (e) clamp the second output terminal to the reference terminal when a voltage across the secondary winding is of the first polarity; and (f) enable recycling of energy between the magnetizing inductance of the transformer and the capacitance between the second output terminal and the reference terminal. The first and second switches may include MOSFETs. The first and second switches may include junction transistors. A first series circuit may have a first resistance connected in parallel with a first unidirectional conducting device. The first series circuit may be connected between the control input of the first switch and the second switch. A second series circuit may have a second resistance and a second unidirectional conducting device connected in parallel and the second series circuit may be connected between the control input of the second switch and the first switch. The first and second switches may include junction transistors. A first integrated semiconductor device formed on a common die may have a plurality of FETs each having a gate, a source, and a drain, and having the same threshold voltage. The first device may have a first switch section and a first clamp section. The first switch section may include one or more of the plurality of FETs connected in parallel. The first clamp section may include one or more of the plurality of FETs. The gates of the FETs in the first switch section and first clamp section may be connected to a first gate terminal. The sources of the FETs in the first switch section and first clamp section may be connected to a first source terminal. The switch circuitry may include a first clamp section. The first clamp section may include a drain terminal connected to a first end of the secondary winding. The first source terminal may be connected to the reference terminal. The first gate terminal may be connected to a second end of the secondary winding. A second switch may be connected between the second end of the secondary winding and the reference terminal. A control input of the second switch may be connected to the first end of the secondary winding. The first clamp section may clamp the first end of the secondary winding to the reference terminal and hold OFF the second switch when the first switch section is ON. A second integrated semiconductor device formed on a common die may include a plurality of FETs each having a gate, a source, and a drain, and having the same threshold voltage. The second device may have a second switch section and a

second clamp section. The second switch section may include one or more of the plurality of FETs connected in parallel. The second clamp section may include one or more of the plurality of FETs. The gates of the FETs in the second switch section and second clamp section may be connected to a second gate terminal. The sources of the FETs in the second switch section and second clamp section may be connected to a second source terminal. The switch circuitry may include the second clamp section. The second gate terminal may be adapted to be clamped by the first clamp and the first gate terminal is adapted to be clamped by the second clamp. The first clamp section may have a drain terminal connected to a first end of the secondary winding. The second clamp section may have a drain terminal connected to a second end of the secondary winding. The first source terminal and second source terminal may be connected to the reference terminal. The first gate terminal may be connected to the second end of the secondary winding. The second gate terminal may be connected to the first end of the secondary winding. The first clamp section may clamp the first end of the secondary winding to the reference terminal and hold OFF the second switch and second clamp sections when the first switch section is ON. The second clamp section may clamp the second end of the secondary winding to the reference terminal and hold OFF the first switch and first clamp sections when the second switch section is ON. The first and second switch sections may drive a power transformer.

In another implementation of the apparatus, the drive circuitry may include a plurality of switches each having a control terminal referenced to a common signal reference for turning the switch ON and OFF and an output connected to drive the transformer. The plurality of switches may include a first switch and a second switch being respectively poled to induce a magnetic flux in the drive transformer in a first and in a second direction when ON. A control circuit may be connected to the control terminals and configured to operate the first and second switches in a series of control cycles each characterized by: (a) two ON intervals during which one of the first and second switches is ON; (b) two OFF intervals during which both of the first and second switches is OFF and energy stored in the drive transformer is used to charge and discharge parasitic output capacitances of the plurality of switches, parasitic capacitances of the switch circuitry, and a parasitic input capacitance of a power switching device having control inputs connected to the first output terminal and the reference terminal.

In another implementation of the apparatus, the drive circuitry may include a plurality of switches each having a control terminal referenced to a common signal reference for turning the

switch ON and OFF and an output connected to drive the transformer. The plurality of switches may include a first switch and a second switch being respectively poled to induce a magnetic flux in the drive transformer in a first and in a second direction when ON. A control circuit may be connected to the control terminals and configured to operate the first and second switches in a series of control cycles each characterized by: (a) two ON intervals during which one of the first and second switches is ON; and (b) two OFF intervals during which both of the first and second switches is OFF and energy stored in the drive transformer is used to charge and discharge parasitic output capacitances of the plurality of switches, parasitic capacitances of the switch circuitry, and parasitic input capacitances of a pair of complementary power switching devices having control inputs connected between the first or second output terminals and the reference terminal. The pair of complementary switching devices may be OFF during a portion of the OFF interval.

In general, another aspect features a method for delivering a unipolar control voltage. A transformer having a primary winding, a secondary winding, and a magnetizing inductance may be provided. Drive circuitry may be provided to drive the primary winding to produce a bipolar voltage across the secondary winding. A first output terminal and a reference terminal may be provided for delivering the control voltage. Switch circuitry may be connected to the secondary winding and adapted to: (a) connect the secondary winding across the first output terminal and the reference terminal when a voltage across the secondary winding is of a first polarity; (b) clamp the first output terminal to the reference terminal when a voltage across the secondary winding is of a second polarity; and (c) enable recycling of energy between the magnetizing inductance of the transformer and the parasitic capacitances of the switch circuitry and the capacitance between the first output terminal and the reference terminal.

In general, another aspect features a method for delivering a unipolar control voltage across a first output terminal and a reference terminal in a circuit using switch circuitry and a transformer having a primary, a secondary winding, and a magnetizing inductance. The primary winding may be driven to produce a bipolar voltage across the secondary winding. The secondary winding may be connected across the first output terminal and the reference terminal when a voltage across the secondary winding is of a first polarity. The first output terminal may be clamped to the reference terminal when a voltage across the secondary winding is of a second polarity. Energy may be recycled between the magnetizing inductance of the transformer and

parasitic capacitances of the switch circuitry and parasitic capacitances between the first output terminal and the reference terminal.

Implementations of the methods may include one or more of the following features. The capacitive load across the first output terminal and reference terminal may include a parasitic gate-source capacitance of MOSFET switch. MOSFETs may be used for the switch circuitry. A first controlled switch having a first control input connected to the first output terminal may be provided. A first switch may be used between a first end of the secondary winding and the reference terminal. A second switch may be used between a second end of the secondary winding and the reference terminal. The first output terminal may be connected to the second end of the secondary winding. A first controlled switch having a first control input connected to the first output terminal may be provided. A control input of the first switch may be connected to the second switch. A control input of the second switch may be connected to the first switch. The first and second switches may have a control threshold which is less than a control threshold of the controlled switch. A second output terminal may be connected to the first end of the secondary winding for delivering a second unipolar control voltage relative to the reference. A second controlled switch may be provided having a second control input connected to the second output terminal. The switch circuitry may be further adapted to: (d) connect the secondary winding across the second output terminal and the reference terminal when a voltage across the secondary winding is of the second polarity; (e) clamp the second output terminal to the reference terminal when a voltage across the secondary winding is of the first polarity; and (f) enable recycling of energy between the magnetizing inductance of the transformer and the capacitance between the second output terminal and the reference terminal. MOSFETs may be used for the first and second switches. Junction transistors may be used for the first and second switches. A first series circuit, having a first resistance connected in parallel with a first unidirectional conducting device, may be connected between the control input of the first switch and the second switch. A second series circuit, having a second resistance connected in parallel with a second unidirectional conducting device, may be connected between the control input of the second switch and the first switch. Junction transistors may be used for the first and second switches. A plurality of switches may be used to drive the transformer. A control terminal of each switch may be connected to reference a common signal reference for turning the switch ON and OFF. A first switch and a second switch in the plurality of switches may be used to

respectively induce a magnetic flux in the drive transformer in a first and in a second direction when ON. The first and second switches may be operated in a series of control cycles each characterized by: (a) two ON intervals during which one of the first and second switches is ON; and (b) two OFF intervals during which both of the first and second switches is OFF and energy stored in the drive transformer is used to charge and discharge parasitic output capacitances of the plurality of switches, the switch circuitry, and a parasitic input capacitance of one or more power switching devices having control inputs connected across the first output terminal and the reference terminal. The drive circuitry may include a plurality of switches to drive the transformer. A control terminal of each switch may be connected to reference a common signal reference for turning the switch ON and OFF. A first switch and a second switch in the plurality of switches may be used to respectively induce a magnetic flux in the transformer in a first and in a second direction when ON. The first and second switches may be operated in a series of control cycles each characterized by: (a) two ON intervals during which one of the first and second switches is ON; and (b) two OFF intervals during which both of the first and second switches is OFF and energy stored in the drive transformer is used to charge and discharge parasitic output capacitances of the plurality of switches, the switch circuitry, and parasitic input capacitances of the first and second controlled switches. The first and second controlled switches may be configured as a pair of complementary power switching devices to drive a power transformer. A sub-interval may be provided during a portion of the OFF interval when the pair of complementary power switching devices is OFF. The first controlled switch and first switch may be integrated onto a first die and each may be provided with the same threshold voltage. The second controlled switch and second switch may be integrated onto a second die and each may be provided with the same threshold voltage.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 shows a DC-DC power converter.

FIGs. 2A and 2B show block diagrams of prior art distributed power architectures.

FIGs. 3A and 3B show block diagrams of examples of the factorized power architecture.

FIG. 4A shows a perspective view of a printed circuit board assembly with a point-of-load DC-DC converter.

FIG. 4B shows a perspective view of a printed circuit board assembly with a point-of-load voltage transformation module.

5 FIG. 4C shows a perspective view of a printed circuit board assembly with a power regulation module and a point-of-load voltage transformation module.

FIG. 5A shows an end view of printed circuit board assemblies incorporating DC-DC converters mounted side-by-side.

10 FIG. 5B shows an end view of printed circuit board assemblies incorporating point-of-load voltage transformation modules mounted side-by-side.

FIG. 6 shows a block diagram of another example of the factorized power architecture.

FIG. 7 shows a block diagram of another example of the factorized power architecture.

FIGs. 8A through 8C show block diagrams of multiple-output power regulators for use in the factorized power architecture.

15 FIG. 9 shows a schematic of a sine amplitude topology for use in a voltage transformation module.

FIGs. 10A through 10H show waveforms for the topology of Fig. 9.

FIG. 11 shows a MOSFET equivalent circuit model.

20 FIG. 12 shows a schematic of an alternate sine amplitude converter topology for use in a voltage transformation module.

FIG. 13 shows a schematic of an alternate sine amplitude converter topology for use in a voltage transformation module.

FIG. 14 shows a schematic of an alternate sine amplitude converter topology for use in a voltage transformation module.

25 FIG. 15A shows a schematic of circuitry using a single secondary winding with full-wave bridge-rectification for use with a sine amplitude topology.

FIG. 15B and 15C show alternate embodiments of output rectification circuitry with synchronous rectifiers for use in a sine amplitude converter topology.

FIG. 16 shows a block diagram of a power regulator for use with an AC input source.

30 FIG. 17 shows a block diagram of a power regulator for use with a DC input source.

FIG. 18 is a block diagram of remote feedback by way of the Power Regulator within the factorized power architecture.

FIG. 19 is a block diagram of remote feedback by way of a PRM within the factorized power architecture.

FIG. 20 is a block diagram of remote feedback by way of a power regulator or PRM from a point-of-load feedback controller.

FIG. 21 shows a partial schematic of alternate circuitry for a sine amplitude converter topology for use in a dual output voltage transformation module.

FIG. 22 shows a schematic of an automatic switch controller.

FIGs. 23A-23D show waveforms for the automatic switch controller of Fig. 22.

FIG. 24 shows a schematic of circuitry for generating a control signal V_s for use with a switch controller in a voltage transformation module.

FIG. 25 shows a schematic of circuitry for current limiting in a sine amplitude converter topology.

FIG. 26 shows a schematic of an equivalent circuit of a sine amplitude converter topology during clamping.

FIGs. 27A and 27B show waveforms for the sine amplitude converter topology of Fig. 25 during clamping.

FIG. 28 shows a schematic of damping circuitry for use in a sine amplitude converter topology.

FIG. 29A shows a block diagram of a buck regulated sine amplitude DC-DC converter.

FIG. 29B shows a block diagram of a boost regulated sine amplitude DC-DC converter.

FIG. 29C shows a block diagram of a buck-boost regulated sine amplitude DC-DC converter.

FIG. 30 shows a block diagram of a bootstrap regulated sine amplitude DC-DC converter.

FIG. 31 is a block diagram of a power-sharing array of VTMs with optional remote feedback to a power regulator or PRM from a point-of-load feedback controller.

FIG. 32 shows a cross section of a transformer structure.

FIG. 33 shows a schematic block diagram of a transformer using the structure of Fig. 32.

FIGs. 34A and 34B show top and bottom perspective views of a sine amplitude converter using the transformer structure of Fig. 32.

FIG. 35 shows a schematic of a SAC converter 302 including a low-loss, common-source gate-drive circuit.

5 FIGs. 36A-36C show waveforms for the converter of Fig. 35.

FIGs. 37A-37H show waveforms for the converter of Fig. 35.

FIG. 38 shows an equivalent circuit of a switch for use in the gate drive circuit of the converter of Fig. 35.

10 FIGs. 39A and 39B show alternative embodiments of switches using discrete components.

FIGs. 40A and 40B show perspective views of an embodiment of the converter of Fig. 35.

FIG. 41 shows a schematic of portion of a converter of the kind illustrated in Figs. 9 and 35 with inter-winding parasitic capacitances.

15 FIG. 42 shows a schematic of an alternative embodiment of a portion of the converter for reducing the effects of the inter-winding parasitic capacitances.

FIG. 43 shows a partial schematic of the low-loss, common-source gate-drive circuitry of the converter of Fig. 35.

FIG. 44 shows a schematic of an alternative low-loss, common-source gate-drive circuit.

20 FIG. 45 shows a schematic of another alternative low-loss, common-source gate-drive circuit.

FIGs. 46A, 46B, 46C show schematics of alternative full-bridge embodiments of a portion of the converter for reducing the effects of inter-winding parasitic capacitances.

25 FIGS. 47A and 47B show, respectively, a schematic and waveform for an isolated gate driver circuit having a bipolar gate control waveform.

FIGS. 48A, 48B and 48C show, respectively, a schematic and waveforms for an isolated gate driver circuit according to the invention having a unipolar gate control waveform.

FIG. 49 shows another embodiment of the gate driver circuit of FIG. 48A for use with complementary MOSFET switches.

30 FIG. 50 shows another embodiment of the gate driver circuit of FIG. 49.

FIG. 51 shows a partial schematic of a SAC comprising output voltage regulation circuitry according to the invention.

FIG. 52 shows a partial schematic of a SAC comprising current limit circuitry according to the invention.

5 FIG. 53 shows an integrated power MOSFET.

FIG. 54 shows a gate driver of the kind shown in FIG. 49 using integrated power MOSFET devices of the kind shown in FIG. 53.

FIGs. 55A and 55B show a DC-DC converter.

FIG. 56 shows a switching power converter feeding a load.

10 FIGs. 57A-57D show waveforms for the circuit of Fig. 56.

FIG. 58 shows an FPA adapted to supply a microprocessor load.

FIGs. 59A, 59B, and 59C show circuit models of a bi-directional VTM.

Like reference symbols in the various drawings indicate like elements.

15 DETAILED DESCRIPTION

A system 20 using the prior art distributed power architecture is shown in Fig. 2A. In the system, a front-end power processor 22 accepts power from an input source 24 and converts it into a bus voltage, V_{bus} , which is distributed over a distance via a distribution bus 26 to a number of separate electronic circuit subassembly PCBs 28a, 28b, 28c...28n, each of which incorporates one or more DC-DC converters, *e.g.*, DC-DC converters 30a...30i. The bus voltage, V_{bus} , is delivered to the inputs of the DC-DC converters 30a...30i and each DC-DC converter delivers regulated output voltages (*e.g.*, voltages V_1 to V_7) for use by circuitry on the subassembly (not shown). Given that DC-DC converters provide a regulation function which enables them to operate over a range of input voltages, the voltage V_{bus} will typically be an unregulated voltage or one which is regulated, but whose value does not control the output voltages (*i.e.*, voltages V_1 to V_7) required by the system.

Another prior art DPA system is shown in Fig. 2B. In the system, an isolated front-end power processor 29 accepts power from an input source 24 and converts it into a bus voltage, V_{bus} , which is distributed over a distance via a distribution bus 26 to a number of separate electronic circuit subassembly PCBs 25a, 25b...25n, each of which incorporates one or more

non-isolated switching regulators, *e.g.*, switching regulators 31a...31e. The bus voltage, V_{bus} , is delivered to the inputs of the switching regulators 31a...31e and each switching regulator delivers a regulated output voltage (*e.g.*, voltages V_1 to V_3) for use by circuitry on the subassembly (not shown). In such a system, the non-isolated switching regulators are sometimes referred to as VRMs ("Voltage Regulator Modules") and one such VRM may be dedicated to power a single integrated circuit device. Given that switching regulators, or VRMs, provide a regulation function which enables them to operate over a range of input voltages, the voltage V_{bus} will typically be an unregulated voltage or one which is regulated, but whose value does not control the output voltages (*i.e.*, voltages V_1 to V_3) required by the system.

In cases in which the input source is an AC utility source, the front-end power processor 22 or the isolated power processor 29 will comprise rectification circuitry for converting the bipolar AC input voltage and current into unipolar form and may also comprise power-factor-correcting circuitry (neither of which are shown in the Figures).

Compared to the CPA architecture, the benefits of the DPA architecture of Figs. 2A and 2B include distribution bus simplicity; flexibility in providing many different load voltages without modifying the underlying power distribution scheme or bus voltage V_{bus} (*i.e.*, by simply providing DC-DC converters with the appropriate output voltages); and minimization of interactions between regulated output voltages owing to variations in loads, bus voltage, distribution bus impedance and related factors.

There are, however, drawbacks to the DPA architecture. In the system of Fig. 2A, for example, incorporation of isolated DC-DC converters onto subassemblies uses up valuable board space; the height of the converters above the subassembly PCB sets a lower limit on spacing between subassemblies and interferes with the flow of cooling air over nearby components; and the DC-DC converters themselves dissipate heat which affects the temperature of nearby components and which must be removed from the region of the subassemblies. Furthermore, if a single DC-DC converter cannot provide adequate power or fault-tolerance for a particular output voltage, multiple DC-DC converters will need to be paralleled, creating additional complexity owing to the need to connect remote sense leads from each paralleled converter to a single, common, point and the need for additional circuitry within each paralleled converter to force power sharing among the units.

These drawbacks are compounded by trends toward higher circuit and systems densities and toward lower system voltages (*e.g.*, to 2V, 1V and below) and the attendant relatively poorer efficiency, and higher dissipation, of the DC-DC converters needed to supply them. While the VRMs of Fig. 2B may have higher power density and efficiency than DC-DC converters, they can create ground-loop problems, owing to their lack of isolation, and they have limited voltage step-down capability (*e.g.*, it is difficult to efficiently generate 1 Volt using a non-isolated VRM when operating from a 48 Volt bus). In either case, a significant compromise in point-of-load power density and efficiency results from the DPA system requirement that DC-DC converters and switching regulators be capable of handling arbitrary voltage transformation ratios and provide regulation over a wide range of input voltages. This architectural requirement forces imbalances in the duty cycles (as defined below) of switching elements and reduced transformer utilization in single stage DC-DC converters, limiting their power density and efficiency.

A system 36 using a new power distribution architecture, called “Factorized Power Architecture” (“FPA”), is shown in Fig. 3A. In the system 36, a front-end power regulator 38 at a first location accepts power from an input source 46 and converts it into a controlled bus voltage at its output, V_f , which is distributed over a distance via a “factorized” distribution bus 40 to a remotely located Voltage Transformation Module (“VTM”) 44. The VTM comprises an isolation transformer (not shown) and transforms the voltage V_f into a voltage V_{out} , for delivery to a load 41. Unlike the DC-DC converters 30 in the DPA of Fig. 2, a VTM in the FPA system may be designed to operate over a tailored, narrow range of input voltages enabling numerous efficiency and power density enhancing features to be deployed. In the preferred VTM architecture discussed in greater detail below, primary and secondary switching elements may be coupled to the primary and secondary windings of the VTM transformer to perform single stage power processing. The VTM may use balanced switching duty cycles in which each primary switching element of a complementary pair is on for essentially the same amount of time as its complement and each secondary switching element of a complementary pair is ON for essentially the same amount of time as its complement. Additionally, the VTM may operate at greater than 90 percent power conversion duty cycle (as defined below) which is indicative of the fraction of each converter operating cycle during which switches in the converter are enabled (as defined below) and power is being transferred from a primary to a secondary of the VTM transformer. The combination of balanced duty cycles and high power conversion duty cycles,

coupled with a short converter operating period, may provide higher power conversion density, efficiency and ease of input/output filtering.

The VTM delivers a DC output voltage, V_{out} , which is a fixed fraction of the voltage, V_{in} , (nominally V_f) delivered to its input. The voltage transformation ratio or voltage gain of the VTM (which may be defined as the ratio, $K = V_{out}/V_{in}$, of its output voltage to its input voltage at a load current) is fixed by design, *e.g.* by the VTM converter topology, its timing architecture and the turns ratio of the transformer included within it. In certain practical implementations without a feedback loop, using non-idealized components, the effective output resistance of the VTM will cause some droop in output voltage as a function of load current as discussed further below. In a typical FPA application, the VTM 44 is placed on a subassembly 42, so that it is close within the subassembly to the load 41 which it powers, and the voltage V_{out} is lower than the voltage V_f so that power loss and voltage drop in the factorized bus 40 are minimized.

Owing to their fixed gain and effective output resistance, VTMs may be paralleled to operate from the same input voltage, V_{in} , nominally V_f , and support a common load, with inherent power sharing attributes. This avoids the need for a power sharing protocol and interface and a multiplicity of remote senses. In applications where the load is itself distributed, *e.g.* across a PCB, multiple VTMs may be separated from each other to remotely deliver individual fractions of the total load current and thus reduce the burden of busing high currents at low voltages, *e.g.* across power planes.

The new Factorized Power Architecture is very flexible. Another configuration of a FPA, system 37, is shown in Fig. 3B. In the Figure, the front-end power regulator 38 of Fig. 3A is factorized into two separate assemblies, a front-end assembly 39 and a power regulator module 43 ("PRM") which may be non-isolated. The front-end assembly accepts power from an input source 46 and converts it into a bus voltage at its output, V_{bus} , which is distributed over a distance via a distribution bus 35 to the input of the PRM. The PRM converts V_{bus} to a controlled voltage, V_f , which is distributed over a distance by the factorized bus 40, to the input of a VTM 44. The VTM 44 provides single-stage power processing through a transformer and switching elements and delivers a DC output voltage, V_{out} , which, for a certain load current, is essentially a fixed fraction of the voltage, V_{in} (nominally V_f) delivered to its input. The PRM 43 may be located relatively far from the front-end power regulator and/or relatively close to the VTM 44. Other VTMs may be powered from the same PRM 43 to operate in parallel with VTM

44, as discussed above, or to provide additional output voltages, as discussed below. VTMs may also be powered from DC output voltages within the power system, including output voltages generated by other VTMs or other types of converters.

The PRM of Figure 3B may be embodied as a buck converter, a boost converter or a buck-boost converter. Likewise, in Figs. 3A and 3B, if the input source 46 is a DC source, the front-end power regulator 38 or the front-end assembly 39 may also be embodied as a buck converter, a boost converter, or a buck-boost converter. A preferred buck-boost DC-DC conversion topology suitable for use as PRMs is described in Vinciarelli, "Buck-Boost DC-DC Switching Power Conversion," U.S. Patent Application No. 10/214,859, filed August 8, 2002, assigned to the same assignee as this application and incorporated by reference.

Some of the benefits of the invention over prior art architectures may be illustrated with reference to Figs. 4A, 4B and 4C. Fig. 4A shows an example of a PCB subassembly 100 for use in a system using the prior art DPA approach. The PCB subassembly may include a DC-DC converter 102 (*e.g.*, the type of modular DC-DC converters manufactured by Vicor Corporation) mounted to a PCB 103, that converts a nominal bus voltage, *e.g.* 48V, (delivered to the card via an edge connector 104) to a 3.3V output and that is rated to deliver up to 150 Watts of power to integrated circuit 105 and, possibly, other electronic circuitry (not shown) on the PCB. The length and width of the DC-DC converter may be 2.28 inch (57.6 mm) and 1.45 inch (36.8 mm), respectively, and its height above the surface of the PCB may be 0.5 inch (12.7 mm). The efficiency of such a converter may typically range up to 90%. Thus, the DC-DC converter may use a PCB area of 3.3 square-inches (21.2 square-cm); occupy 1.65 cubic-inches (26.9 cubic-cm) of volume; and, at its full rated load of 150 Watts, exhibit a power density of 91 Watts/cubic-inch (5.6 Watts/cubic-cm) and dissipate more than 16 Watts of heat into the environment of the subassembly 100.

Fig. 4B shows an example of a PCB subassembly 110 for use in a system using the FPA shown in Fig. 3A. Every aspect of the PCB subassembly 110 is the same as that of the PCB subassembly 100 of Fig. 4A, except that the PCB subassembly 110 of Fig. 4B incorporates a VTM 108 instead of a DC-DC converter. A VTM operating in the FPA system can be made smaller than a DC-DC converter of equivalent output power, and therefore occupies less volume and its height above the surface of the PCB subassembly may be lower. For example, a VTM for converting a controlled 48V bus voltage to deliver up to 150 Watts at 3.3V output may be fit into

a package (e.g., an IC sized package) measuring approximately 1.35 inch (34.3 mm) square and approximately 0.2 inch (5.1 mm) high over the surface of the PCB. The peak efficiency of such a VTM within its normal operating range may be approximately 96%. Thus, the VTM may use a PCB area of 1.82 square-inches (11.8 square-cm); occupy 0.36 cubic-inches (6.0 cubic-cm) of volume; and, at its full rated load of 150 Watts, exhibit a power density of 416 Watts/cubic-inch (25.0 Watts/cubic-cm) and dissipate only 6 Watts of heat into the environment of the subassembly 110.

Fig. 4C shows an example of a PCB subassembly 113 for use in a system using the factorized power architecture shown in Fig. 3B. Every aspect of the PCB subassembly 113 is the same as that of the PCB subassembly 100 of Fig. 4A, except that the PCB subassembly 113 of Fig. 4C incorporates a VTM 108 and a PRM 107 instead of a DC-DC converter. By separating the PRM from the VTM, a source of heat may be removed from the point of load and higher power density may be achieved at the point of load with easy to manufacture, cost-effective components.

As shown by the examples of Figs. 4B and 4C, the VTM (or PRM and VTM) of the FPA requires significantly less area on the PCB subassembly 110 than the DC-DC converter of the DPA system, leaving more board area for electronic circuitry. The VTM (or PRM and VTM) dissipates significantly less power, easing cooling requirements for the assembly 110 (113). Thermal management is also made easier because the lower height of the VTM 108 (or PRM 107 and VTM 108) above the surface of the board offers less interference to airflow over nearby components. The reduction in height of the VTM (or PRM and VTM) relative to the DC-DC converter also allows PCB subassemblies to be mounted closer together in a system, thereby affording an improvement in overall system density. For example, Figs. 5A and 5B show end views of groups of several PCB subassemblies as they might appear when mounted side-by-side within a rack mounted electronic system (not shown). Fig. 5A shows the PCB subassemblies 100 of Fig. 4A. Fig. 5B shows the PCB subassemblies 110 of Fig. 4B. Assuming, in each instance, that the DC-DC converters 102 and VTMs 108 are the tallest components on their respective subassemblies 100, 110, then the pitch, D2, between the PCB subassemblies of Fig. 5B can be made 0.3 inch (7.6 mm) smaller than the pitch, D1, between the PCB subassemblies of Fig. 5A, thus potentially doubling system density.

Alternate embodiments of the FPA are shown in Figures 6, 7 and 8. In Figure 6 the system 50 is an expanded version of the system 36 of Fig. 3. A front-end power regulator 38 accepts power from an input source 46 and converts it into a controlled bus voltage, V_f , at its output which is distributed over a distance via a factorized distribution bus 40 to a number of separate electronic circuit subassembly PCBs 42a through 42n, each of which incorporates one or more VTMs, *e.g.*, VTMs 44a through 44g. The VTMs provide load voltages (*e.g.*, voltages V_1 to V_7) that power loads (not shown) on the subassembly PCBs. In addition to VTMs, the subassembly PCBs may contain DC-DC converters (*e.g.*, DC-DC converter 48) and/or Switching Regulators (*e.g.*, Switching Regulator 65) and/or Charge Pumps (not shown) to provide certain output voltages.

Fig. 7 shows an example of an FPA system in which a multiple-output power regulator 62 delivers three different controlled bus voltages V_{f1} , V_{f2} , and V_{f3} to three factorized distribution buses 40a, 40b, and 40c. Each of the three factorized buses is connected to one or more subassemblies. In the Figure, the controlled voltage V_{f1} is delivered to a first factorized bus 40a, which distributes power to VTMs 64a-64d on subassemblies 42a and 42b; the controlled voltage V_{f2} is delivered to a second factorized bus 40b, which distributes power to VTMs 68a-68d on subassemblies 42c and 42d; and the controlled voltage V_{f3} is delivered to a third factorized bus 40c, which distributes power to VTMs 66a-66g on subassemblies 42e, 42f, and 42g. In addition to VTMs, the subassemblies may contain DC-DC converters (*e.g.*, DC-DC converter 48) and/or Switching Regulators (*e.g.*, Switching Regulator 65) and/or Charge Pumps (not shown) to provide certain output voltages.

The multiple-output power regulator 62 of Fig. 7 may be embodied in different structures, some examples of which are illustrated in Figs. 8A, 8B, and 8C. In Fig. 8A, a multiple-output power regulator 62 consists of a multiple output switching regulator that operates off of a single input source 46 and delivers controlled outputs, V_{f1} , V_{f2} , V_{f3} , for delivery to factorized distribution buses. In Fig. 8B, a multi-output regulator 62 comprises several independent power converters 63a, 63b, 63c, which operate off of a single input source 46. Each of the converters delivers a controlled output for delivery to a factorized distribution bus. In Figs. 8A and 8B the input sources may be either AC or DC sources. In Fig. 8C, the multi-output regulator comprises independent regulators 66a, 66b, 66c which operate off of one or more different input sources. For example, independent regulator 66a operates off of two sources 45,

47, one of which might be an AC source and the other a DC source, such as a battery backup source. The other two independent regulators 66b, 66c are shown operating from independent sources 49, 51. These and a wide variety of other combinations of sources and regulating power supplies can be configured to generate one or more controlled bus voltages for distribution in a FPA system.

Application of FPA is not limited to rack mounted electronic systems. For example, with vehicular electrical power consumption increasing, there has been a trend toward higher bus voltages in vehicles, such as the emerging 42 Volt bus standard in automotive power systems. Factorized power architecture is a cost-effective, lightweight, and energy-efficient solution for providing point-of-load conversion in such applications (*e.g.*, to efficiently power 12 volt loads from a 42 V factorized bus). Other examples of applications which will benefit from the density and efficiency advantages of the FPA may be identified in other markets for electronic products, including, in particular, consumer, medical, industrial and military products.

A DC-DC converter in a prior art DPA system includes power train and control circuitry for regulating the output voltage as the converter input voltage varies over a relatively wide range (*e.g.*, the maximum input operating voltage is typically 2 or more times the minimum input operating voltage) and requires use of components which are capable of operation at full rated load over the entire input voltage range. Specifically, regulation circuitry takes up space in the converter and therefore reduces power density relative to a device without regulation circuitry. As significantly, the characteristics of power train components needed to accept a relatively wide input operating voltage range also reduce power density and efficiency. For example, in certain types of single stage power converters, output rectifiers must be selected to withstand peak voltages associated with operation at maximum input operating voltage and, at the same time, be able to carry an unbalanced share of the load. Primary-side switching elements need to be selected using similar constraints and the presence of significant dead times, during which power is not delivered across the transformer adds to the burden of these elements. In order to simultaneously satisfy both high current and high voltage requirements, switching elements require a large semiconductor die, which will exhibit higher parasitic capacitance and switching losses. If, instead, a smaller die is used, conduction losses will be higher. The ability to accommodate large changes in input voltage also compromises the size or efficiency of energy storage or reactive components, such as transformers.

In DC-DC converters in which a DC-to-DC transformer stage is cascaded with a pre-regulator, voltage and current stresses on rectifiers and switches in the DC-to-DC transformer stage are limited owing to the constancy of the voltage delivered by the pre-regulator, but the components in the pre-regulator must be selected to accept wide input voltage variations and the combination of the pre-regulator with the DC-to-DC transformer stage reduces the power density of the unit. Thus, in cascaded DC-DC converters, as in single stage converters, operation over a wide input voltage range generally translates into limited power density and efficiency at the point-of-load.

In general, the power density, efficiency, and flexibility of a point-of-load power converter, and the power-sharing performance of paralleled arrays of such converters, may be improved by factorizing away the power conversion functions associated with voltage regulation and by providing only essential functions at the point-of-load, such as voltage transformation and/or isolation. Assuming comparable switching frequencies with comparable power conversion topologies and timing architectures, the adoption of the Factorized Power Architecture, may double the power density and efficiency of point-of-load converters relative to the prior art Distributed Power Architecture. VTMs may also provide greater overall performance (*e.g.*, bandwidth), scalability (*e.g.*, inherent power sharing) and reliability (*e.g.*, lower complexity, fault tolerance) at a significantly lower cost per Watt delivered to the point-of-load. These advances may be achieved by optimizing power conversion topologies and timing architectures for use within the VTM.

Although a VTM for use in a FPA system can be based upon any prior art DC-to-DC transformer topology, certain VTM topologies may be superior to others with respect to performance characteristics, including: power density, conversion efficiency, output impedance and “droop” (*i.e.*, variations in output voltage with variations in loading), transient response, radiated noise, and conducted emissions at input and output. High power density and conversion efficiency may be achieved in both half-bridge and full-bridge pulse width modulated (“PWM”) topologies by incorporating a ZVS architecture. However, the equivalent circuit of a PWM converter includes the total equivalent series resistance of the circuit plus the impedance of a leakage inductance component serially interposed between the input source and the load. Mweene, *ibid.* In a VTM, this impedance would impair the VTM open-loop regulation by

causing the output voltage to droop as the load is increased (by, *e.g.*, 5%, or more, as the load varied over its full range).

Similarly, high efficiency and power density can be achieved with Frequency Modulated (“FM”) quasi-resonant or resonant converter topologies by incorporating a ZCS timing architecture at frequencies below resonance or, alternatively, a ZVS timing architecture at frequencies above resonance. However, here too, the equivalent circuit includes the total equivalent series resistance of the circuit plus the capacitive or inductive impedance of the resonant circuit at the operating frequency. In both cases, with PWM and FM converter topologies, the output impedance of the converter, and its droop characteristics, are degraded by the presence of reactive impedance standing in the way of achieving the low output impedance preferred for a VTM.

A preferred converter topology and timing architecture for the VTMs of the FPA, which will be generally referred to as a Sine Amplitude Converter (“SAC”) topology, has many advantages over prior art DC-to-DC transformer topologies. The SAC topology is nominally operated at resonance so that the reactive impedances of the elements of the resonant tank cancel each other out. The SAC uses a resonant topology at resonance so that the impedance of the resonant circuit becomes essentially resistive, minimizing the output impedance and open-loop resistance of the converter, and thus minimizing open-loop voltage droop as a function of changing load. Greater consistency in open-loop DC output resistance, owing to the elimination of dependency on reactive impedances, gives rise to fault tolerant power sharing attributes which are particularly desirable in applications in which multiple, paralleled, VTMs are operated as a power sharing array.

SAC converters are capable of essentially pure sinusoidal waveforms, thus optimizing spectral purity, and hence the converter’s conducted and radiated noise characteristics. The SAC control architecture adapts to varying output loads by varying the amplitudes of the voltage and current waveforms while preserving the essentially sinusoidal character of the resonant components. The timing architecture of the SAC topology supports ZVS operation of the primary switches and ZCS and ZVS operation of the secondary switches, virtually eliminating switching losses in the primary switching elements and secondary switching elements, or rectifiers, particularly synchronous rectifiers, enabling higher switching frequencies and higher converter power density and efficiency. Sine Amplitude Converters provide the best

combination of attributes to support the requirements of VTMs and high performance DC-DC converters.

A first SAC topology 90 is shown in Fig. 9. This topology, incorporating a sine amplitude control architecture, enables high operating efficiency, high power density, low noise and low output impedance. In Fig. 9, the SAC comprises a half-bridge series resonant converter controlled by a switch controller 130. Power is delivered to the SAC at an input voltage V_{in} and is delivered to a load 120 at a voltage V_{out} . The half-bridge resonant converter comprises primary switches 58 and 60; a resonant circuit including resonant capacitors 32 and 34 of value $C_R/2$ (resulting in an equivalent total resonant capacitance equal to C_R) and resonant inductor 74, of value L_R ; and transformer 70, with primary winding 71 and center-tapped secondary winding 72. In general, the resonant inductance L_R may comprise, in whole or in part, the leakage inductance of the transformer 70. As discussed below, in preferred embodiments the resonant inductance 74 may consist entirely of the transformer leakage inductance. The magnetizing inductance of the transformer may be set to a relatively low value to facilitate energy-recycling and efficient ZVS operation. For switching frequencies above 1 MHz, the effective permeability of the transformer core may be below 100, allowing selection of low-loss ferrite materials. The characteristic resonant frequency of the resonant circuit, and thus the series-resonant converter, is $f_R = 1/(2\pi \sqrt{C_R * L_R})$. A full-wave rectifier, comprising diodes 52 and 54, may be connected between the secondary winding 72 and the storage capacitor 56 and load 120. Storage capacitor 56 integrates the pulsating current I_o and smoothes the voltage across the load, V_{out} . As further described below, the switch controller 130 operates the switches so that the SAC 90 operates at an essentially constant switching frequency over its normal range of loads. The controller's timing architecture provides ZVS operation of the primary switches and ZCS and ZVS operation of the secondary switches.

Steady state operation is explained with reference to Figure 9 and the waveforms of Figure 10. The primary switches 58 and 60 may be MOSFET devices (or alternative devices, e.g., GaAs power switches), which, as illustrated in Fig. 11, may comprise a body diode 122 and parasitic capacitance 120. Signals delivered to the gate terminal 124 of the MOSFET (by the switch controller 130) control the conductivity of the MOSFET channel (currents in the body diode 122 and parasitic capacitance 120 are not under control of the gate terminal). The storage capacitor 56 is sufficiently large so that the voltage across it is essentially constant and equal to

V_{out} throughout each converter operating cycle. Voltage drops in switches and diodes, when conducting, are assumed to be zero for part of this analysis. The turns ratio of the transformer, which is the number of secondary turns divided by the number of primary turns, is N_s/N_p . The input voltage, V_{in} , is assumed to be constant. As used herein, the terms “closed,” “ON” and “enabled,” as applied to a switch, mean that the switch is enabled to conduct current which it could otherwise block and the terms “open,” “OFF” and “disabled” mean that a switch is not ON. As defined herein, the term “duty cycle,” as applied to a switch in a switching power converter, is defined as the fraction of the converter operating cycle during which the switch is enabled.

In steady state operation, the average value of V_c will be nominally $V_{in}/2$ (*i.e.*, one half of the SAC input voltage, V_{in}). The converter uses a series of converter operating cycles (*e.g.*, converter operating cycle t_0 - t_4 in Fig. 10) to convert power from the input for delivery to the output. During each power transfer interval (*e.g.*, time periods t_0 to t_1 and t_2 to t_3 in Fig. 10) the resonant circuit is driven (by primary switches 58, 60) with an equivalent voltage source equal essentially to $V_{in}/2$. A short energy-recycling interval may follow each power transfer interval to allow recycling of energy stored in capacitive elements and a reduction in switching losses. As shown in Fig. 10, the converter operating cycles have a period (*i.e.*, the converter operating period, $T_{op} = t_4 - t_0$), that is nominally greater than the characteristic resonant period, $T_R = 2\pi * \sqrt{C_R * L_R}$, in an amount equal to the sum of the durations of the energy-recycling intervals.

At time t_0 , switch 58 is closed (Fig. 10A) by the switch controller 130. Between times t_0 and t_1 , a current, I_{s1} (Fig. 10C), flows in the circuit formed by switch 58, transformer primary 71, resonant inductance 74 and resonant capacitors 32 and 34. As shown in Fig. 10C, the current I_{s1} comprises a resonant portion, I_r , which rises and falls essentially sinusoidally at the characteristic resonant frequency, f_R , and a magnetizing current portion, the peak-to-peak fluctuation of which is approximately equal to $V_{in} * (t_1 - t_0) / (2 * L_M)$, where V_{in} is the SAC input voltage and L_M is the magnetizing inductance of the transformer 70. During the interval t_0 through t_1 the current in the resonant inductance, I_L (Fig. 10F), is essentially equal to I_{s1} .

At time t_1 , the value of the resonant portion of the current I_{s1} returns to zero, the secondary rectifier current I_s is essentially zero and switch 58 is opened by the switch controller 130, ending the power transfer interval. During an energy-recycling interval, with switches 58 and 60 open (*e.g.*, intervals t_1 - t_2 and t_3 - t_4 in Fig. 10), the transformer magnetizing current may be

used to charge and discharge the parasitic capacitances of the switches (e.g., capacitance 120, Fig. 11) and other circuit parasitic capacitances, causing the voltage V_{sw} across switch 60 (Fig. 10E) to be reduced. The rate of change of voltage across the disabled switch during the energy-recycling interval increases in inverse proportion to the magnetizing inductance of the transformer. If the magnetizing current is sufficiently large and the time duration of the energy-recycling interval is sufficiently long, the voltage across the switch may be driven to zero (or essentially zero) volts for ZVS, as shown in Fig. 10E at time t_2 . Should the energy-recycling interval extend beyond the time necessary to allow the voltage to be reduced to zero, the body diode 122 (Fig. 11) of switch 60 will carry the transformer magnetizing current until switch 60 is turned ON, thereby holding the switch voltage nominally at zero volts. In the case where the controller maintains energy-recycling intervals long enough for ZVS, the energy-recycling intervals may be referred to as ZVS intervals. Given that the ON time of the primary switches is essentially independent of load and that the SAC input voltage is essentially constant, the peak magnitude of the magnetizing current at the ends of the power transfer intervals will also be essentially fixed and independent of load. Therefore, the length of the energy-recycling interval necessary to allow the switch voltage to reach zero will also be essentially independent of load, and ZVS may be achieved using an energy-recycling interval of constant duration.

At time t_2 , switch 60 is turned ON (Fig. 10B) by the switch controller 130. Because the voltage across switch 60 is reduced relative to V_{in} , or, for sufficiently low values of magnetizing inductance and long energy-recycling intervals, essentially zero, and because the secondary rectifier current is essentially zero at turn ON and turn OFF, both primary and secondary switching losses are essentially eliminated. Operation of the SAC 90 between times t_2 and t_3 is the same as between times t_0 and t_1 , except that a reverse current (I_{s2} , Fig. 10D) flows in inductor 74 and switch 60. The mirroring of magnetizing current during the second power transfer interval, t_2 - t_3 , resets the core of the transformer.

At time t_3 the value of the resonant portion of the current I_{s2} returns essentially to zero and switch 60 is opened by the switch controller 130. During the energy-recycling interval, between times t_3 and t_4 , both switches 58 and 60 are OFF and the flow of magnetizing current will charge and discharge parasitic capacitances so that the subsequent turn ON of switch 58, at time t_4 , can also be accomplished essentially without loss, thus completing a full cycle.

Use of magnetizing current to effect ZVS of primary switches upon essential completion of the resonant half cycles allows commutation of secondary switching elements, or rectifiers, at essentially zero current and zero voltage without substantial increase of the root mean square (“RMS”) current (and conduction losses) in primary switches. The essentially sinusoidal variation of the current I_L and the AC component of the voltage V_c are illustrated in Figs. 10F and 10H, respectively. Fig. 10G shows the rectified current, I_o , which is delivered to the storage capacitor 56 and the load 120. The storage capacitor 56 is sufficiently large so that the voltage across it may be considered to be essentially constant throughout an operating cycle of the SAC 90. The SAC 90 responds to changes in load resistance and load current with corresponding changes in the amplitude of the resonant current, I_p , and thus the amplitude of the current through primary and secondary switching elements. Conduction losses are therefore minimized under all load conditions.

The SAC operates at a high power conversion duty cycle (where the term “power conversion duty cycle” means the fraction of the operating cycle during which switches are ON and power is being transferred from the input of the SAC to the load, *i.e.*, in Fig. 10 the sum of the power transfer intervals, $(t_1-t_0) + (t_3-t_2)$, divided by the duration of the operating cycle, (t_4-t_0)) and using balanced duty cycles (the power transfer interval using switch 58, interval t_0-t_1 , is essentially equal to the power transfer interval using switch 60, interval t_2-t_3). For example, in a SAC having a characteristic resonant frequency of 1.5 Megahertz, the total duration of the two power transfer intervals will be 667 nanoseconds and each energy-recycling interval (assuming a selection of transformer magnetizing inductance low enough to rapidly slew the parasitic capacitances of MOSFET switches) may be approximately 20 nanoseconds, resulting in a total operating cycle of 707 nanoseconds and power conversion duty cycle of 94%. Thus, a SAC according to the invention can be expected to achieve power conversion duty cycles greater than 80% and, for optimized units, power conversion duty cycles greater than 90%. At lower operating frequencies, power conversion duty cycles approaching 100% are possible.

The virtual elimination of switching losses (due to primary ZVS and secondary ZCS and ZVS operation), minimization of conduction losses under all load conditions (due to amplitude modulation), constant (resonant) frequency operation, reduction or elimination of filter components (due to spectral purity of the sine wave), and high switching frequency contribute to

the high efficiency and high power density realizable using the Sine Amplitude Converter topology 90.

One way of controlling the switches in the SAC is to turn them ON and OFF using signals whose frequency, relative timing and ON and OFF intervals are pre-determined. This, however, requires that the relative timing of the switch control signals be adjusted to compensate for variations in the characteristic resonant frequency due, for example, to component value variations in individual units. A preferred way to control the switches is to provide an “automatic switch controller” which automatically turns the switches OFF at times when the sinusoidal component of the currents I_{s1} and I_{s2} (Figs. 10C, 10D) returns essentially to zero and which provides an energy-recycling interval sufficient for ZVS at each switch transition prior to turning the complementary switch ON. The benefits of using an automatic switch controller include minimization of switching and conduction losses and maximization of converter efficiency; elimination of timing adjustments in individual SAC units due to variations in values of circuit elements resulting from component tolerances; optimization in current sharing accuracy among SACs in a parallel array, as discussed below; optimization of soft switching, *i.e.* primary ZVS and secondary ZCS and ZVS; and maximization of the spectral purity of the sinusoidal waveforms in the converter.

An embodiment of an automatic switch controller 179, for controlling the switches in a SAC, is shown in Fig. 22. Operation of the circuit will be explained with reference to the SAC schematic of Fig. 9 and the waveforms of Fig. 23. In Fig. 22, the signal V_s may be a voltage proportional to the primary current, I_L , in transformer 70. As shown in Fig. 23A, and as discussed above with respect to Figs. 10C and 10D, the signal V_s may include a sinusoidal component and a magnetizing current component. In Fig. 23A, the sinusoidal component of V_s goes to zero at times t_A , t_B , t_C , and t_D which are the times at which the magnetizing current (as indicated by the dashed line) reaches its peak values. In Fig. 22, the signal, V_N (Fig. 23D), at the negative input of comparator 170, is the sum of a portion of the signal V_s and a portion of the signal V_{cont} (Fig. 23C) at the output of the comparator. The relative contributions of V_s and V_{cont} may be determined by the relative values of resistors 172 and 174. The ratio of resistors 172 and 174 is selected so that the contributions of V_{cont} and V_s offset and cancel each other at times t_A , t_B , t_C , and t_D , thereby causing the signal V_{cont} to transition between positive and negative values at those times. To improve convergence, resistor 174 may be replaced by an inductor (not

shown) to provide a time-dependant ramp instead of a fixed offset. Signal V_{cont} may be fed back to the positive input of comparator 170 via capacitor 178 and resistor 176. This positive feedback may ensure fast transitions in the signal V_{cont} without signal bounce. The values of capacitor 178 and resistor 176 may be chosen so that the signal V_P (Fig. 23C) returns to a value of essentially zero volts prior to the next switching transition.

With reference to Figs. 9 and 23, when the signal V_{cont} is positive, switch control circuitry 180 may cause switch 58 to be enabled, and when the signal V_{cont} is negative, the switch control circuitry 180 may cause switch 60 to be enabled. Switch control circuitry 180 may also include delay circuitry (not shown) to set the energy-recycling intervals during which both of the switches 58 and 60 are OFF, as discussed above. After one switch is turned OFF, the complementary switch may be turned ON after the end of an energy-recycling interval (*e.g.*, in Fig. 10, the ends of the energy-recycling intervals are at times t_2 , t_4 , and t_6). The duration of the energy-recycling intervals may be pre-determined (*e.g.*, by using RC time constants to generate delays) or the end of each interval may be triggered by sensing when the voltage V_{sw} (Fig. 10E) is at or near zero volts for S2 or at or near V_{in} for S1.

The signal V_s may be generated by sensing the variations in flux in the core of the transformer 70, as taught in U. S. Patent No. 5,659,460, entitled "Switch Control in Quantized Power Converters," assigned to the same assignee as this application, and incorporated in its entirety by reference. Another way to generate the signal V_s is shown in Fig. 24. In the Figure, a primary winding 181 of a current transformer 182 is connected in series with the primary winding 71 of the SAC transformer 70. The voltage V_s is generated by the flow of the transformed current I_s , from the secondary winding 183 of the current transformer, in resistor 184. Current transformers may also be used to sense current in the secondary winding 72 of the SAC transformer 70.

Current flow in secondary windings of SAC transformers may also be sensed by monitoring voltages across secondary synchronous rectifiers in series with secondary windings. At the completion of power transfer intervals, as currents in synchronous rectifiers approach zero, voltages across synchronous rectifiers falling below a voltage threshold (*e.g.* 10 mV) may be used to trigger the turn-OFF of the gates of MOSFET switches used for synchronous rectification and to trigger the turn-OFF of corresponding primary switches. Thus, in an alternative embodiment, an automatic switch controller turns OFF primary switches at times

when currents in secondary windings return to zero and essentially coincident with the turn-OFF of corresponding secondary switches, and turns ON complementary primary switches after a delay, to provide for an energy-recycling interval. This embodiment of an automatic switch controller requires fast communication (i.e., approximately 5 nS for a 1 MHz converter) across the secondary-to-primary isolation boundary, *e.g.* by the use of pulse transformers, but avoids the need for precise subtraction of magnetizing current which is inherent to primary-side controllers, such as that shown in Fig. 22.

Alternate embodiments of SACs are shown in Figs. 12, 13, and 14. Fig. 12 shows a full-bridge SAC 92. Operation of the circuit is similar to that of the converter of Fig. 9, except that the switch controller 140 controls a total of four MOSFET switches 55, 57, 59, and 61. With reference to Figs. 12 and 10, switches 55 and 61 are turned ON and OFF with the timing shown in Fig. 10A (for switch 58) and switches 57 and 59 are turned ON and OFF with the timing shown in Fig. 10B (for switch 60). During each half-cycle of oscillation, the resonant circuit (*i.e.*, the series circuit comprising resonant inductance 74, which may consist totally or partially of the leakage inductance of transformer 70, and resonant capacitor, 33) is driven by an equivalent voltage source equal to V_{in} and each of the switches in the circuit of Fig. 12 blocks a voltage V_{in} when OFF.

Fig. 13 shows an alternate embodiment of the sine amplitude converter of Fig. 9 using a single resonant capacitor 33. Fig. 14 shows another embodiment of a sine amplitude converter having a resonant frequency set by resonant capacitor 33 and inductance 74. The resonant inductance 74 may totally or partially consist of the leakage inductance of transformer 70 and may be small relative to the inductance of input inductor 142. A distinguishing attribute of the topology of Fig. 14 is that the two primary switches have a common node.

Referring to Fig. 15A, an untapped secondary winding 73 and full-wave rectifier 53 may be used as an alternative to the center-tapped secondary winding 72 and rectifier 52 and 54 configuration shown in Figs. 9, 12, 13, and 14. A drawback of the configuration of Fig. 15A is that two rectifiers conduct during each half-cycle, increasing total rectifier conduction losses particularly at low output voltages.

Although synchronous rectifiers have been used to reduce rectifier conduction losses in the output circuitry of conventional switching power converters, their use typically requires limiting the converter operating frequency to contain switching losses. In non-zero current

switching converters, high current slew rates in the synchronous rectifier FETs may give rise to significant switching losses from either delayed or premature turn-OFF of the FET conduction channel, thereby limiting high frequency operation. The ZCS architecture and the sinusoidal character of the current waveform on the secondary side of sine amplitude converters, however, translate into essentially zero current and limited current slew rates at the turn-ON and turn-OFF transitions of the secondary switching elements, which greatly relaxes timing constraints in the switching of synchronous rectifiers. This in turn enables switching at or near zero current and minimizing switching losses even at high operating frequencies. Synchronous rectifiers, when used in the SACs, come without the switching loss penalties associated with other converter topologies, and help reduce power losses in the output circuitry of any of the SAC embodiments at frequencies higher than 1 MHz and as much as an order of magnitude greater than practical with conventional converters, thus allowing further increases in power density and efficiency.

Referring, for example, to Fig. 15B, "smart-synchronous-rectifier" devices 75 and 77 (*e.g.*, of the kind described in U.S. Patent Application No. 09/499,822, "Active Rectifier," assigned to the same assignee as this application and incorporated by reference in its entirety) may be used in place of the rectifiers 52 and 54 of Figs. 9, 12, 13 and 14.

An additional embodiment with synchronous rectifiers is shown in Fig. 15C. After a secondary switch, *e.g.*, a MOSFET synchronous rectifier, in the SAC is turned OFF, the voltage across the secondary windings reverses, causing a possible overshoot in the voltage across the MOSFET synchronous rectifier switch being turned OFF (*e.g.* switches 162, 164). The overshoot is a result of ringing between energy stored in the leakage inductance associated with the secondary winding 72 (labeled in the Fig. 15C as " L_{RS} " beside each half of the winding) and circuit parasitic capacitances (*e.g.*, the parasitic capacitance of the synchronous rectifier switches, not shown in the figure). The ringing may be dampened using a dissipative snubber circuit. Referring to Fig. 15C, an improved approach for controlling the synchronous rectifier switches is shown. Each recycling circuit 153 and 155 in the pair comprises a capacitor 150 and 156, a resistor 152 and 158, and a rectifier 175 and 173. The recycling circuits 153 and 155 are connected between a respective end 157, 159 of the transformer secondary winding 72 and the gate control input of a respective MOSFET synchronous rectifier switch which is connected to the other end of the winding. Rectifiers 166 and 168 may be discrete devices or the body drain diodes of MOSFETs 162 and 164. A comparator 154, 160, connected to the gate control input of

a respective MOSFET 162 and 160, turns the MOSFET OFF when the voltage across the MOSFET (e.g., voltage V_{FET}) is negative and releases the gate control input to an open-circuit condition when the voltage across the MOSFET is positive. In operation, when the polarity of the voltage at end 157 (159) of the secondary 72 goes from positive to negative (negative to positive), MOSFET switch 162 is turned OFF (MOSFET 164 is released). Energy which would otherwise cause ringing in the voltage across MOSFET 162 may instead be delivered to the gate capacitance (not shown) of MOSFET 164 via the recycling circuit 153, thereby turning ON MOSFET 164 and preventing ringing in the voltage across MOSFET 162. Thus, the secondary switches, comparators and recycling circuits of Fig. 15C are discrete implementations of “smart-rectifier-snubber” (“SRS”) devices which reduce dissipation by recycling energy into the gates of the MOSFET switches 162, 164 in order to turn the switches ON while incorporating active circuitry to rapidly turn the switches OFF at essentially zero current. The comparator and MOSFET elements of SRS devices are particularly well suited to silicon integration to improve turn-OFF speed and overall performance at a reduced cost. SRS devices may also be coupled to auxiliary secondary windings to optimize the gate voltages applied to the MOSFET switches. Given that SACs operate from controlled input voltages in the FPA resulting in controlled voltages across the transformer windings, SRS devices provide efficient synchronous rectifiers for SACs.

In the sine amplitude converters of Figs. 9, 12, 13 and 14, the peak-to-peak sinusoidal variations in I_L and V_C in steady state operation are dependent on and vary with the value of the load current I_{out} . An increase or decrease in the load will cause a corresponding increase or decrease in the peak value of I_L and the peak-to-peak value of V_c . Neglecting rise and fall times associated with ZVS delays and assuming operation at resonant frequency, the peak primary resonant current $I_L = I_p$ is approximately given by:

$$I_p = I_{out} * (\pi * N_s / (2 * N_p)),$$

and the peak-to-peak resonant voltage, ΔV , is approximately given by:

$$\Delta V = 2 * V_p = I_{out} * (\pi * N_s / N_p) * \text{sqrt}(L_R / C_R),$$

where I_p and V_p are as illustrated in Figure 10; where N_p and N_s represent the number of turns of the primary and each secondary winding, respectively; and where L_R is the primary resonant inductance and C_R is the resonant capacitance.

Under similar assumptions and further assuming that: a) the primary and secondary switching elements have ON state resistances R_{sp} and R_{ss} , respectively, b) the transformer has a primary and secondary equivalent series resistance R_{tp} and R_{ts} , respectively, and c) neglecting other loss terms, the output voltage, V_{out} , is approximately given by:

$$V_{out} = V_{in} * (N_s/N_p) - (\pi^2/8) * [(R_{ts} + R_{ss}) + (R_{tp} + R_{sp}) * (N_s/N_p)^2] * I_{out},$$

and the converter's open-loop output resistance is approximately given by:

$$R_{out} = (\pi^2/8) * [(R_{ts} + R_{ss}) + (R_{tp} + R_{sp}) * (N_s/N_p)^2].$$

In the absence of any compensating feedback, this output resistance will cause voltage droop at the point-of-load as a function of load. However, due to the nature of a Sine Amplitude

Converter topology and the consequent absence of droop due to complex impedance terms, particularly leakage inductance, the droop is significantly reduced relative to other topologies or control architectures. Low open-loop output resistance is advantageous to improved regulation in multiple output VTMs or in a FPA system deploying multiple VTMs powered from the same bus voltage, V_f . Low open-loop output resistance is also advantageous under closed-loop operation if feedback is provided to the PRM, since it diminishes the slew rate required of the bus voltage, V_f , which may then be bypassed by substantial amounts of capacitance to provide point-of-load energy storage at the input of a VTM. Up to their bandwidth, VTMs will then provide an energy reservoir by reflecting to the point of load an effective hold up capacitance as the inverse of the square of the VTM gain K , or voltage transformation ratio, multiplied by the input capacitance. Thus, VTMs incorporating a SAC topology are capable of improved dynamic performance with, or without, the benefit of closed-loop operation.

The open loop output resistance of a SAC or, in general, a VTM may be modified by controlling the operation of the VTM using a load-dependent control variable. For example, the output current may be used to increase or decrease output resistance by adjusting the VTM switching frequency and/or the duty cycle of switches and/or the phase of the switches as a function of output current. A reduction in the output resistance of the VTM due to feedback from the VTM input or output current, or other control variable, may be used to improve VTM output voltage regulation as a function of load and VTM dynamic performance under stepped loads, independently of feedback provided to the PRM and without the limitations of point-of-load voltage-driven, closed-loop operation. Alternatively, the output current may be used to

increase output resistance by controlling the ON-state resistance of primary or secondary switching elements as a function of input or output current.

It should be noted that the switch, winding, and other ohmic resistances that contribute to the open-loop output resistance, R_{out} , of a SAC have positive temperature-coefficients. Because of this overall positive temperature-coefficient and the underlying positive resistance, R_{out} , of a SAC, the outputs of two or more SACs may be connected in parallel, as a means of increasing the total power which may be delivered to a load, and the SACs will automatically share in the power delivered to the load. Current sharing is independent of individual resonant frequencies, as long as the operating frequency of each SAC is locked to its respective resonant frequency. The worst case error in current sharing among paralleled SACs of equivalent construction and power rating is simply limited to the worst case mismatch in the total output resistance, R_{out} , of each SAC and is mitigated by the positive temperature-coefficient of R_{out} . Assuming a worst case model variability in R_{out} of 10%, inherent current sharing to an accuracy better than 10% may be achieved, without the need for additional complex circuitry and power sharing interfaces to force current sharing among SACs. Current and power sharing accuracy may be improved further by supplementing the open-loop output resistance by current-driven feedback as described above.

In the absence of closed-loop regulation of the output voltage, this current sharing mechanism comes, as others before it, at the expense of droop in the output voltage with increasing load. However, if the output voltage of an array of paralleled SACs is regulated by feedback controlling the input voltage to the SAC array (*e.g.*, as shown for a more general array of VTMs in Fig. 31), good regulation and current sharing may be achieved without the need for dedicated power sharing circuitry and fault prone interfaces. These desirable paralleling attributes may be retained in fault tolerant applications with an OR'ing diode added in series with the output of each SAC, if the OR'ing diode function is incorporated by use of a FET switch with positive temperature-coefficient resistance. Fault tolerance at the input of a SAC may also be achieved by incorporating a FET and a control circuit that turns the FET OFF to disconnect the SAC from the input bus under abnormal conditions.

The presence of inductive impedances (*e.g.*, parasitic inductances and transformer leakage inductance) in switching circuits of PWM converters has generally been viewed as undesirable because the high-frequency oscillatory ringing associated with such inductances (in combination with parasitic capacitances of the switches, windings and other circuit components)

causes increased component stresses; generates radiated electromagnetic interference and conducted noise; and generally requires use of dissipative “snubber” circuits to provide damping. Thus, prior art PWM converters have traditionally been designed as “low-Q” circuits, in which leakage inductances of transformers and other parasitic inductances are minimized.

5 Transformers for PWM converters have therefore traditionally been constructed with interleaved windings, which increase inter-winding coupling and minimize leakage inductance and which also reduce the equivalent series resistance of the transformer by minimizing proximity effects in the windings. On the other hand, resonant converters have traditionally been designed with the opposite viewpoint: the prior art has taught the use of “high-Q” circuits in such converters, since
10 it was deemed desirable to maximize the recovery of energy stored in resonant tank elements. Thus, transformers in resonant converters have been typically designed with non-interleaved windings as a means of providing transformer leakage inductance as all or part of the resonant inductance, a first order circuit element dictated by the energy storage requirements of resonant converters.

15 Although the use of “high-Q” circuits in resonant converters seems intuitively satisfying, it does not necessarily result in the most efficient converter if the topology does not impose a requirement of intermediate energy storage in the resonant tank. Design of a “high-Q” transformer provides an increase in transformer leakage inductance at the expense of an increase in transformer equivalent series resistance. In other words, the techniques used to construct such
20 “high Q” transformers result in higher values of equivalent resistance than would be present in a “low-Q” transformer design (*e.g.*, one designed for a PWM converter). This is because the “high-Q” techniques that result in a lower coupling coefficient and higher leakage inductance (*e.g.*, non-interleaved windings) also result in increased loss due to skin and proximity effects, causing a reduction in the effective utilization of the winding cross-section.

25 The “quality factor,” Q , of a series resonant converter operating at resonance is defined herein as $Q = Z_L / R_{eq}$, where $Z_L = 1/(2\pi * f_R * L_R)$ is the total inductive impedance of the resonant circuit at the resonant frequency, f_R ; where the inductance L_R includes all discrete, leakage and circuit parasitic inductances, reflected to the transformer primary and in series with the resonant circuit; and where R_{eq} is the total equivalent series resistance of the circuit, reflected
30 to the transformer primary and including, resistances of windings, ON-state resistances of switches, rectifiers and resonant capacitors, measured at 27 °C with a 10 mA AC test current.

Since a SAC relies on principles of resonant charge transfer, as opposed to resonant energy transfer, the power throughput of a SAC at a given switching frequency does not uniquely define an energy storage requirement for its resonant elements, L_R and C_R . The inductance L_R (or the corresponding impedance at the resonant frequency) therefore represents a “spare” degree of freedom, which may be used to optimize converter efficiency and bandwidth. The quality factor, Q , does not directly reflect cycle-by-cycle losses in a SAC. Rather the losses in the resonant tank of a SAC are directly proportional to the total equivalent series resistance R_{eq} .

Given the physics of losses in a transformer, minimization of R_{eq} does not entail maximization of Q . Thus, preferred embodiments of a SAC are those in which the equivalent series resistance R_{eq} is minimized. For such embodiments, the transformer is generally designed to minimize leakage inductance; no external resonant inductance is used; and the values of the resonant capacitors are chosen to set the characteristic resonant frequency of the converter. In contrast to typical prior art series resonant converters having Q values of the order of 30, a preferred embodiment of a SAC will have a Q of less than 13. Q factors below 10 are possible and support higher conversion efficiency.

Since Q is proportional to reactive impedance and intermediate, serial energy storage, a low- Q resonant circuit may also generally provide higher bandwidth and shorter transient response time, together with greater inherent stability. The transient response time is defined as the time interval from an instantaneous step change in output load current (which causes the steady-state output voltage to change in an amount, ΔV , and to settle to a final steady-state value, V_{ss}) to when the output voltage settles into a band which is $\pm 0.1 \Delta V$ wide and centered around V_{ss} . A lower Q results in a corresponding reduction in the peak energy stored in the resonant inductor for a given load current. Whereas, for a given frequency, the capacitance of the resonant circuit increases in inverse proportion to the resonant inductance, corresponding reductions in peak voltages across the resonant capacitor reduce the peak energy stored in the capacitor in inverse proportion to the capacitance for a given load current. Thus, under stepped load conditions, a SAC with lower Q , lower resonant inductance and higher resonant capacitance is subjected to a smaller change in cumulative resonant energy. Since the number of converter cycles required to effect a change in cumulative resonant energy grows with the magnitude of the change, lower Q results in a more “nimble” SAC, capable of responding to stepped loads in fewer converter cycles and, therefore, faster. The reduced time lag in the time domain translates

in reduced phase lag in the frequency domain and improved stability for lower Q values. However, the value of Q is constrained from below by waveform distortion due to circuit damping, particularly at reduced output loads.

Depending on the load range required of a VTM, Q values as low as 3, or lower, are practical. With such low Q values, SACs respond to virtually instantaneous changes in output load within a few converter cycles and slew their output current to minimize or, for low enough Q , totally eliminate voltage overshoot at the point-of-load under stepped load conditions. Specifically, with the SAC topology of Fig. 9 operated at a resonant frequency of 2 MHz with a $Q = 3$, a VTM with an output voltage of 3.3V is capable of responding to a load step from zero to 50A within 0.5 microseconds. This represents an improvement in transient response time and bandwidth greater than an order of magnitude relative to best-of-class contemporary DC-DC converters. It also represents better transient performance than VRMs, which are often operated as a paralleled phased array (frequency “interleaved”) to enhance their bandwidth in order to meet the demanding dynamic needs of leading edge microprocessors.

Thus, VTMs incorporating a SAC topology with a low Q resonant circuit provide significantly higher bandwidth, power density, efficiency and high current scalability than contemporary point-of-load VRMs. The greater performance of VTMs results from the combination of the Factorized Power Architecture and the attributes of high frequency, low Q , Sine Amplitude Converters. The relative simplicity, reliability and cost also point to VTMs, as opposed to VRM arrays, as the preferable point-of-load converters for future, state-of-the-art microprocessors.

Successive generations of contemporary microprocessors have trended towards lower regulated operating voltages, higher speeds and higher currents, thereby requiring that their closed-loop power supplies exhibit higher bandwidth and greatly increased stepped load current handling capability. A preferred approach for satisfying these large transient current demands using the FPA avoids the need for an extremely fast closed-loop response without requiring large storage capacitors at the point of load to supply the load current over a long time scale commensurate with the response time of a relatively slower control loop.

Figure 56 shows a typical switching power supply 501 supplying power to a load 41 at a load voltage $V_L = V_o$ with a storage capacitor 502 connected across the load. Figures 57A through 57D show waveforms illustrating the general response of such a system to a step change

in load current, I_L , assuming that the input voltage, V_{in} , is constant. In Figure 57A, the load current makes a step change from a value I_1 to a value I_2 at time t_0 . Because the switching power supply 501 has a finite response time (owing, e.g., either to the inertia of energy storing elements, such as output chokes, in the power supply, or to the response time associated with closed-loop control of the output voltage), the output current, I_o , delivered by the switching power supply cannot change instantaneously to satisfy the increased current demand of the load as shown in Fig. 57B. Referring to Figs. 57B and 57C, the storage capacitor 502 supplies the difference between the load current, I_L , and the output current, I_o , supplied by the switching power supply 501. At time, t_0 , the capacitor current, I_C , will equal the increase in load current $I_C = I_2 - I_1$. For simplicity, effects of equivalent-series-resistance and equivalent-series-inductance associated with the storage capacitor 502 have been ignored in the waveforms of Figure 57. In practice, selection of appropriate capacitors, or combinations of capacitors, and attention to implementation of low-impedance interconnections between the capacitor(s) and the load 41, are important factors.

After time t_0 , the output current, I_o , delivered by the switching power supply begins to increase and the capacitor current, I_C , begins to decrease. The response time of the change in output current, I_o , is a function of the characteristic time constant, T_c , of the switching power supply circuitry and capacitor 502. The characteristic time constant may, for example, be associated with the dominant pole in the transfer function of the system comprising the switching power supply and the capacitor. During the time period (t_0 - t_1) that the capacitor is supplying current to the load, the voltage, V_L , across the capacitor and the load decreases, as shown in Figure 57D. At time t_1 , the output current I_o equals the load current I_L , discharging of the capacitor ceases ($I_C=0$), and the output voltage V_L is at a minimum, *i.e.*, the deviation of the load voltage, ΔV_L , from the nominal load voltage V_L as a result of the increase in load current is at a maximum. After time t_1 , the switching power supply supplies an output current, I_o , exceeding I_2 (*i.e.*, the output current supplies the load current, I_2 , and replenishes the charge withdrawn from the capacitor during the previous interval, t_0 - t_1).

If the system of Fig. 56 operates “closed-loop” (e.g., the switching power supply 501 comprises a closed-loop output voltage regulation scheme), the voltage V_L will return to a value close to V_o after time t_1 ; if the system operates “open-loop” (e.g., the switching power supply 501 is of the kind which does not comprise a closed-loop output voltage regulation scheme, such

as a DC-to-DC transformer) the voltage V_L will approach a value that is less than V_o , owing to the finite output resistance of the switching power supply. The deviation in the load voltage, ΔV_L (Fig. 57D), in response to the step change in load is a function of the magnitude of the change in load current, the capacitance, C_S , of the storage capacitor, and the characteristic time constant, T_c . A requirement that the load voltage, V_L , not deviate by more than an amount ΔV_L in response to a step change in load current, ΔI_L , can dictate large capacitance values at the point of load or unreasonably high power supply bandwidth requirements.

A system 508 for achieving a desired load voltage response while significantly relaxing the bandwidth required of the closed loop that sets the average load voltage and also avoiding excessively large capacitors at the point of load, is shown in Figure 58. The system 508 employs the FPA for powering rapidly varying loads, such as a contemporary high-speed microprocessor. The system 508 comprises a PRM 503, which may include a switching power supply, and a VTM 505, which may include a SAC. The VTM 505 has a voltage transformation ratio, $K = V_{out}/V_{in}$, where V_{in} is the VTM input voltage (the factorized bus voltage, V_f , supplied by the PRM in Fig. 58) and V_{out} is the VTM output voltage, ($V_o = V_L$ delivered to the load). A storage capacitor, 506 is connected across the load 41 and a storage capacitor 504 is connected across the input of the VTM. A measurement indicative of the value of the load voltage, V_L , is supplied to a feedback input 507 on the PRM 503 as a means of maintaining the voltage V_L at some, essentially constant, predetermined value. As explained above in connection with Figs. 56 and 57, the deviation in the VTM output voltage, ΔV_{L1} , in response to a step change in load current, will be a function of the magnitude of the change in load current, the capacitance, C_1 , of the storage capacitor, and the characteristic time constant T_{VTM} of the VTM. Because the VTM input voltage, $V_{in} = V_f$ is supplied by a power supply (PRM 503) which also has a finite response time, T_{PRM} , the deviation in the VTM output voltage will also be a function of the extent to which its input voltage, V_f , varies.

The system strategy in Fig. 58 scales capacitors 506 and 504, time constants of the PRM, T_{PRM} , and VTM, T_{VTM} , and the voltage transformation ratio, K , to achieve the desired response and to ease the bandwidth requirements and the capacitance at the point of load. The underlying principle relies on the greater energy storage density of higher voltage capacitors and the relatively high open loop bandwidth that can be achieved with certain kinds of VTMs, such as SACs. By storing energy at the input of a VTM having a voltage transformation ratio K , the

capacitance required to hold sufficient energy to supply a load power requirement over a time scale T_{VTM} with an acceptable voltage deviation at the load, is reduced by a factor of K^2 relative to the amount of capacitance that would be required directly across the load. The relative ease of energy storage at higher voltages coupled with the high open-loop bandwidth and low output impedance of certain VTMs (*e.g.*, SACs) can be used to significantly relax the bandwidth required of the closed loop that sets the average load voltage ($T_{VTM} < T_{PRM}$). In essence, from the point of view of the load, the system strategy makes the equivalent output impedance of the power supply appear to the load to be very low (*e.g.*, essentially equal to that of the VTM alone) irrespective of the transient response or output impedance of the upstream, closed-loop, PRM power supply. The overall system, as described, can provide very high performance with rapidly changing loads, even if the PRM is a conventional power supply with substantial inertia owing to the presence of internal energy storage elements.

By way of example, certain loads, such as contemporary microprocessors, operate from relatively low voltage supplies (*e.g.*, less than one volt DC) and draw very rapid and large current steps (*e.g.*, in excess of one hundred Amperes). However, because the load voltage is so low, the sudden step in load power is relatively small (*e.g.*, one hundred Watts) and can be supplied by a VTM having a low output impedance up to a frequency high enough to minimize the amount of capacitance required at the microprocessor. This capacitance, 506 (Fig. 58), is made large enough to support the microprocessor current requirement within a time scale, T_1 , which is preferably greater than or equal to the characteristic open-loop response time constant of the VTM by itself, T_{VTM} . More specifically, capacitor 506 is chosen to prevent the load voltage, V_L , from deviating more than an amount ΔV_{L1} in response to a step change in load current, ΔI_L (or, in general, to a change in load current which occurs over a time period which is short in comparison to the response time of the VTM, T_{VTM}).

The capacitance at the input of the VTM, 504 (Fig. 58), is made large enough to support the microprocessor current requirement within a time scale, T_2 , which is preferably greater than or equal to the closed-loop response time of the upstream voltage regulator (*e.g.*, PRM 503 in Fig. 58). In particular, capacitor 504 is chosen to prevent the factorized bus voltage, V_f , in Fig. 58, from deviating more than an amount ΔV_f in response to a step change in load current, ΔI_L (or, in general, to a change in load current which occurs over a time period which is short in

comparison to the response time of the PRM 503, T_{PRM}). As a result, the upstream regulator closed loop bandwidth requirement may be relaxed to a relatively longer time scale.

Consider an example, with reference to Fig. 58, in which the load 41 is a microprocessor requiring a 1 Volt supply ($V_o=1.0V$); the factorized bus voltage V_f is 48 Volts; the VTM voltage transformation ratio, K is $1/48$; the response time of the VTM, $T_{VTM} \leq 1 \mu S$; and the response time of the PRM, $T_{PRM} \leq 10 \mu S$. Setting the first time scale, T_1 to $1 \mu S$ ($T_1 \geq T_{VTM}$) and a maximum output voltage deviation for T_1 , ΔV_{L1} , to 100 mV for a 100 Amp step change in load current, ($\Delta V_{L1} = 100 \text{ mV} @ T_1$ for $\Delta I_L = 100A$), the capacitor 506 at the point of load should have a minimum capacitance:

$$\begin{aligned} C_1 &= (\Delta I_L * T_1) / \Delta V_{L1} \\ C_1 &= (100A * 1 \mu S) / 100 \text{ mV} \\ C_1 &= 1,000 \mu F. \end{aligned}$$

Setting the capacitor 504 at the input of the VTM may be done with greater flexibility. The maximum deviation of the VTM input voltage, ΔV_F , at time T_2 is reflected as a deviation at the output of the VTM, ΔV_{L2} , equal to $\Delta V_F * K$ (ignoring the VTM output resistance, R_{out}). Thus ΔV_F may be chosen by setting $\Delta V_{L2} = \Delta V_{L1}$ (yielding $\Delta V_F = \Delta V_{L1}/K$) or more robustly by setting $\Delta V_{L2} < \Delta V_{L1}$ with little additional cost because the net gain in capacitance reduction for a given hold up time is $1/K^2$ (2,304 for $K=1/48$). Continuing with the example, the second time scale, T_2 may be set to $10 \mu S$ ($T_2 \geq T_{PRM}$), and the maximum input voltage deviation, ΔV_F may be set to 4.8Volts ($\Delta V_F = \Delta V_{L1} / K$), in which case the capacitor 504 at the input of the VTM should have a minimum capacitance:

$$\begin{aligned} C_2 &= ((\Delta I_L * K) * T_2) / (\Delta V_f) \text{ or using } \Delta V_f = \Delta V_{L2}/K \\ C_2 &= (\Delta I_L * K^2 * T_2) / (\Delta V_L) \\ C_2 &= (100A * (1/48)^2 * 10 \mu S) / (0.1V) \\ C_2 &= 4.3 \mu F. \end{aligned}$$

A more robust design choice (allowing for a voltage drop due to the VTM output resistance, R_{out}) may be to set ΔV_F to .21 Volts (which results in $\Delta V_{L2} = \Delta V_f * K = .21/48 = 4.4mV$ at T_2), in which case the capacitor 504 at the input of the VTM should have a minimum capacitance:

$$\begin{aligned} C_2 &= (\Delta I_L * K * T_2) / (\Delta V_f) \\ C_2 &= (100A * (1/48) * 10 \mu S) / 0.21V \end{aligned}$$

$$C_2 = 99 \mu\text{F}.$$

Thus a VTM with a sufficiently low open loop output resistance can support a 100 Amp step change in load current for over 10 μS with only 100 μF of input capacitance due to its current gain of 48 and its voltage gain of 1/48. The net gain in capacitance reduction for a given hold up time is $1/K^2 = 48^2 = 2,304$.

By extending the time scale, T_{PRM} , required of the closed loop control system, the power delivery system to the load can be made simpler, more efficient and cost effective. The open loop output resistance, R_{out} , of the VTM may also be used to provide all or part of Automatic Voltage Positioning ("AVP"), an Intel requirement to manage the voltage at the microprocessor as a function of the microprocessor load. This requirement is addressed in its entirety by closed loop control under the existing microprocessor power paradigm.

In addition to exhibiting a well-behaved and predictable response to sudden increases in load current demand, the power system may, in certain applications, also need to be able to manage output voltage excursions associated with sudden decreases in load current. For example, in contemporary digital systems comprising high-speed microprocessors, logic and memory, current consumption can decrease from essentially full load to no-load virtually instantaneously. Despite these severe "load dump" conditions, the power supply output voltages must remain within predictable, relatively narrow, limits.

The "load dump" problem is usually caused by inductive inertia within the power supply. The amount of energy stored in inductive elements (e.g., output filter inductors) in a power supply increases as the current delivered to the load increases. When the load current is suddenly interrupted, some or all of the excess inductive energy stored in the power supply will flow out toward the load. This results in energy being "dumped" into output storage capacitors, with a corresponding transient increase in load voltage. Output over voltage under load dump conditions is a potential problem with any power supply having inductive inertia. For a given load, however, a SAC with a "low Q" resonant circuit (as defined herein) will have relatively lower inductive inertia compared to a conventional switching power supply and will therefore exhibit relatively lower output voltage deviation under load dump conditions.

VTMs, specifically SAC converters, incorporating synchronous rectification on the secondary side of the VTM transformer are capable of processing power "backwards", from their output back to their input. In other words, they can both source current to the load and sink

current away from the load. This is so because the FET switches that provide synchronous rectification by conducting "channel" current in the direction of their "body-drain" diode, may also conduct channel current in the opposite direction. As a result, whenever the VTM output voltage exceeds the input voltage multiplied by K (as defined above), power will flow from the VTM (SAC) output to the input. This reverse current flow is driven by an incrementally increased output voltage (associated with the "load dump" of energy from the VTM out to the load) and limited by an effective resistance, such as the output resistance of the VTM (SAC). Except for attendant losses, similar to the losses occurring in "normal" forward power flow, reverse power flow is efficient: energy taken from the VTM output is delivered to the VTM (SAC) input, except for incidental losses, such as the loss in parasitic circuit resistances, due to reverse power processing.

Bi-directional power flow, coupled with the high open loop bandwidth of VTMs (SACs) and a high voltage step down ratio, as enabled by the isolation transformer in a VTM (SAC), are essential ingredients in providing power to low voltage, high current systems, such as, for example, contemporary digital systems comprising high-speed microprocessors. Bi-directional VTMs (SACs) are capable of supporting the escalating trend in such systems (and others) towards lower voltages and higher currents, and are uniquely capable of responding to virtually instantaneous load surges and load "dumps" while efficiently maintaining the load voltage within a narrow range of desired values.

A circuit model 600 of a bi-directional VTM, shown in Figure 59A, may be constructed by combining 3 standard SPICE components: 1) a "Voltage Controlled Voltage Source" (VCVS) 604 with a transformation ratio K; 2) a "Current Controlled Current Source" (CCCS) 609 with a transformation ratio K; and 3) a resistor 614 of value R_{out} . The VCVS accepts an input voltage V_i at its input terminals 605, 606 and produces an output voltage, $V_s = K * V_i$, at its output terminals 607, 608. The VCVS has infinite input impedance and zero output impedance. A current I_i flowing between the input terminals 610, 611 of the CCCS causes a current $I_s = K * I_i$ to flow between CCCS output terminals 612, 613. There is zero impedance between the input terminals of the CCCS. In the model 600, the VCVS input voltage V_i equals the VTM input voltage V_{in} and the CCCS input current I_i equals the VTM output current I_{out} . The VCVS senses, at its input terminals 605, 606, the voltage, V_{in} , at the input of the VTM and generates a voltage at its output terminals 607, 608 equal to $K * V_{in}$. The CCCS senses, between its input terminals

610, 611, the output current of the VTM, I_{out} , and causes a current equal to $K \cdot I_{out}$ to be drawn from VTM input source, thus conserving total power. The resistor R_{out} , in series with the VTM output, represents the primary mechanism of power conversion losses and defines the open loop VTM output resistance. Given the duality between the voltage and current sources, the model
 5 600 is bi-directional and capable of fully characterizing a VTM as a $V \cdot I$ converter, except for delays owing to the finite VTM switching frequency and, specifically, the Q of the SAC (higher Q causes larger delays). The model of Fig. 59A may be modified to include the latter effects by addition of an inductance 616 and resistance 617, of appropriate values, as shown in Fig. 59B.

A further refinement to the models of Figs. 59A and 59B is shown in Fig. 59C, in which
 10 input and output filter components, and associated and other circuit parasitics, have been added to form an essentially complete model of a VTM. Input filter components comprise input inductor L_{in} 622 (which includes any parasitic inductance associated with the input connections) and input filter capacitor C_{in} 620 with its associated equivalent series resistance R_{Cin} 621. Output filter components comprise output filter capacitor C_{out} 624 with its associated equivalent series
 15 resistance R_{Cout} 625. Inductance L_{out} 626 models the (small) parasitic inductance associated with the converter output connections. A current source 623, of value I_Q , models the current drawn by control circuitry within the VTM.

Transformer windings may be physically interleaved by use, *e.g.*, of multi-layer PCB construction techniques. Having optimized the windings to minimize their equivalent series
 20 resistance at the desired SAC resonant frequency and having measured the typical transformer leakage inductance of a certain design, the resonant frequency may then be “tuned in” for a particular product line by selecting an appropriate value for the resonant capacitors. Manufacturing process variations affecting leakage inductance will only impact the resonant frequency as a square root function of the inductance. Thus, for example, a 10% variation in
 25 leakage inductance will only cause a 5% change in resonant frequency and a 5% change in peak-to-peak voltage in the resonant capacitor. More significantly, such a variation does not affect the voltage or current ratings of any of the semiconductor switches or diodes. In any case, to achieve a particular characteristic frequency, $f_R = 1/(2\pi \cdot \sqrt{C_R \cdot L_R})$, the value of one of the two elements which determine f_R (*i.e.*, C_R or L_R), can be measured for each VTM; the other value
 30 calculated from the formula for f_R ; and the requisite complementary component selected and installed. For example, in one embodiment of a SAC, the leakage inductance of the transformer

(which is the total resonant inductance, L_R , in the circuit) can be measured, the value of C_R calculated, and a capacitor (or capacitors) with a value closest to the calculated value can be retrieved from a store of capacitors of different values. This method avoids the need to manufacture transformers, particularly multi-layer PCB transformers, having tightly controlled values of leakage inductance in order to manufacture SACs of a given resonant frequency. Alternatively, in another embodiment of a SAC, the leakage inductance of a PCB transformer may be complemented by an incremental resonant inductor, which may be selected from a store of inductors, to achieve the desired value of total resonant inductance within an acceptable tolerance range.

To provide sufficient magnetizing current to achieve ZVS of the primary switches of a SAC within a short energy-recycling interval, to achieve a high power-conversion duty cycle, the magnetizing inductance of the SAC transformer needs to be set to a sufficiently low value. For example, for the SAC topology of FIG. 9, assuming a low magnetizing inductance and that the total parasitic capacitance reflected at the primary switching node, V_{sw} , can be approximated by a fixed capacitor of capacitance C_{sw} , the duration of an energy-recycling interval, T_m , to achieve complete non-dissipative charge and discharge of parasitic capacitances would be approximately:

$$T_m = (C_{sw} * V_{in}) / [V_{in} * \pi * \sqrt{(L_R * C_R) / (2 * L_M)}] = 4 * C_{sw} * L_M / [\pi * \sqrt{(L_R * C_R)}].$$

Requiring that the energy-recycling interval be relatively short, so as to achieve a high power conversion duty cycle, i.e. greater than 90%, then leads to the following approximate requirement for the transformer's primary magnetizing inductance:

$$L_M < (1/4) * (C_R / C_{sw}) * L_R, \text{ or}$$

$$L_M < 1 / (16 * \pi^2 * C_{sw} * f_R^2),$$

where f_R is the converter's resonant frequency. Assuming that the bulk of C_{sw} is due to parasitics in the silicon of the switching elements (e.g. FETs), it can then be seen that, for a given semiconductor (FET) technology, the magnetizing inductance to provide ZVS may need to be reduced in inverse proportion to the square of the resonant frequency. At high frequencies, i.e. above 1 MHz, and given contemporary FET technology, this leads to the use of transformers with relatively low magnetizing inductance and low transformer core effective permeability.

In a specific example, a VTM was modeled with the SAC half-bridge topology of FIG. 9 and with a transformation ratio, K , equal to 1/20 to provide 3.3 Volt at up 150 Watts from a factorized bus at a voltage, V_f , approximately equal to 70 V. The primary switches, 58 and 60,

were 40 m Ω FETs. The secondary rectifiers, 52 and 54, were 1.2 m Ω FETs operated as synchronous rectifiers. The resonant capacitance, C_R , was 52,000 pF and the resonant inductance, L_R , was 200 nH, setting the resonant frequency to approximately 1.5 MHz. The transformer turns ratio was 10:1. The transformer core was ferrite with a 0.63 square cm cross
 5 section, a 3.15 cm magnetic path length and a 0.45 cm gap, resulting in a low magnetizing inductance, L_M , of approximately 2 μ H and an effective permeability of only 7. The energy-recycling interval was approximately 20 nS and the power conversion duty cycle was approximately 94%. The power train efficiency reached a peak of approximately 96%.

Given the relatively low values of effective permeability achieved above, transformer
 10 core materials for SACs operating at high frequencies, *e.g.* above 1 MHz, may be selected from low initial permeability, low-loss ferrites or other high frequency permeable media. Initial permeabilities in the range of 5 to 500 (as opposed to the initial permeabilities of typical MnZn “high frequency” ferrites in the range of 500 to 3000) may be adequate, providing flexibility in the optimization of core materials to minimize core loss and in the geometry and construction of
 15 the transformer.

A transformer structure of the kind shown in Figures 32 and 33, referred to herein as a “dog’s bones” transformer may be used in a SAC. The dog’s bones transformer may be used to achieve the high transformation ratios needed to provide the low output voltages and high currents required by present and future microprocessors cost-effectively. A multiplicity of
 20 cylindrical permeable core element sets (two such sets 221a, 221b are shown in Fig. 32, each set comprising a core piece 222a, 222b and an end piece; 224a, 224b each set representing a permeable dog’s bone) are inserted into cylindrical holes 225a, 225b of a multi-layer PCB. In Fig. 32 the PCB comprises primary winding conductive etches 226a, 226b and secondary winding conductive etches 228a, 228b on non-conductive substrate layers 229a, 229b, 229c. As
 25 shown in the Figure, each exemplary primary winding consists of two sets of primary etches, each set consisting of three turns, one set being located between substrates 229a and 229b and the other set being located between substrates 229b and 229c. As shown in Fig. 33, the two primaries 226a, 226b may be connected in series. In Figs. 32 and 33, the exemplary secondary windings 228a and 228b each comprise a pair of etches, one forming a single turn on the outer
 30 surface of substrate 229a and the other a single turn on the outer surface of substrate 229c. The two single turns in each pair may be connected in parallel, as shown in Figure 33, to form a

composite single turn of relatively high current capacity. The secondary windings may be used independently to power separate SAC outputs or they may be connected either in series or in parallel (thereby, in the example shown in the figures, forming, respectively, either a 2 turn winding or single turn winding of relatively high current capacity). Thus, for the winding example shown in Fig. 33, turns ratios of either 6:1 or 12:1 may be achieved. Smaller turns ratios may be achieved by connecting the primary windings in parallel.

The orientation of windings associated with neighboring dog's bones may be poled in opposite orientations as indicated by arrows 195 and 197 in Fig. 32 showing flux paths within the dog's bones, so that some of the magnetic flux of each dog's bone is returned within neighboring dog's bones. The relatively close proximity of the edges of the magnetic core pieces and end pieces allows magnetic flux from individual core elements (*e.g.*, 222a, 222b) to be coupled to neighboring elements at a distance above and below the PCB, thereby reducing stray magnetic fields and losses due to proximity effects in the windings. Gaps between neighboring elements may be filled with a permeable medium to further minimize the interaction of magnetic fields with windings and reduce proximity losses. The use of gaps outside of the PCB, as distinct from gaps within holes in the PCB (which are characteristic of PCB transformers), is advantageous by providing a reduction in PCB transformer losses.

The dog's bones transformer core structure may also be implemented using a variety of alternative core element geometries (two of which are described below), or it may be implemented without the use of discrete core elements by over-molding the PCB with a permeable medium. The relatively low magnetizing inductance and effective permeability requirements of high frequency SAC transformers allows for the permeable medium to have a relatively low initial permeability, *e.g.* 10, which may be obtained by loading the composition of an over-mold resin with finely ground ferrite powder. This provides a means to reduce core loss per unit volume at high frequency and flux levels relative to conventional high initial permeability MnZn or NiZn ferrites.

Figures 34A and 34B, show, respectively, top and bottom perspective views 240a, 240b of a SAC embodiment that includes an embodiment of a transformer of the kind shown in Figs. 32 and 33. The transformer 251 has four core element sets, each set comprising one of four core pieces 222a-222d and one of four end pieces 224a-224d. Etches forming the windings (not shown) are part of multi-layer PCB 242. MOSFET switches 248, packaged in 5mm x 5mm

square MLP packages, may be used for the primary switches and may be connected to the primary windings of the transformer via etches (not shown) on the PCB 242. The control circuitry, which may include, *e.g.*, an automatic controller of the kind described above with reference to Figures 22 and 23 or in the discussion of alternative embodiments, may be provided within an integrated circuit 244. The gates of each of the MOSFET switches-248 may be driven by primary gate driver circuits 246, which may receive turn-on and turn-off command information from the control circuit 244 via galvanically isolated transformers 254, and which may operate as described in Vinciarelli, U.S. Patent No. 6,107,860, "High Efficiency Floating Gate Driver Circuit Using Leakage-Inductance Transformer," assigned to the same assignee as this application and incorporated by reference in its entirety. MOSFET switches 250, packaged in 5mm x 5mm square MLP packages, may be used for the secondary-side synchronous rectifiers and may be controlled by synchronous gate drivers 252, which may be of the kind described in Vinciarelli, U.S. Patent Application No. 09/499,822, assigned to the same assignee as this application and incorporated by reference in its entirety. Resonant capacitors 300, in conjunction with the leakage inductance of the transformer structure, set the characteristic resonant frequency of the converter. Input capacitors 256 provide a reservoir of energy and input filtering. The outputs of the synchronous rectifiers 250 connect to output capacitors 258, 260. In the example shown in Figs. 34A and 34B, the secondary windings associated with core sets 222a and 222b may be connected via two of the four synchronous rectifiers to capacitors 258, and the secondary windings associated with core sets 222c and 222d may be connected via the other two synchronous rectifiers to capacitors 260, to deliver two separate, isolated and filtered DC output voltages, V_1 and V_2 , at terminal pairs 262a, 262b and 264a, 264b, respectively. The two voltage outputs, V_1 and V_2 may be the same and the terminals 262, 264 may be connected in parallel to provide a single output with increased total power output; or the voltages may be the same or different and may be used separately. The input voltage, V_{in} , may be delivered to the SAC 240 at input terminals 266a, 266b. A signal terminal 268 may be used to deliver a feedback signal to a PRM or power regulator front end, or it may be used for another purpose, *e.g.*, as an enable/disable input to control the outputs of the SAC. The overall dimensions of the SAC 240, including the over-molding epoxy (discussed below), may be $L = 1$ inch (25.4 mm), $W = 1$ inch (25.4 mm) and $H = 0.2$ inch (5mm). A SAC of the kind shown in the Figs. 34A and 34B may

deliver 3.3 Volts at up to 100 Watts operating at a frequency of 1.5 MHz and with a conversion efficiency of 96 % achieving a power density of 500 watts per cubic inch.

Because of the relatively low value of effective permeability required of a SAC transformer core, mechanical-stress induced cracks in the core will have relatively little effect on transformer performance. This makes the overall VTM assembly compatible with being over-molded as an integrated circuit. Removal of heat from the over-molded package is simplified by placing the switching elements, which generate most of the heat, on the top side of the assembly, as shown in Fig. 34A. Thus, the entire assembly 240 of Figures 34A and 34B may be over-molded with thermally conductive epoxy (*e.g.*, Novolac resin, manufactured by Epoxy Systems, Inc., Jericho, Vermont, USA)(not shown in the Figure).

In application within a FPA distributed power system, a SAC is typically operated at an essentially constant input voltage. The switches, rectifiers and other components, therefore, are subjected to well-defined stresses and may be selected to optimize both power density and efficiency. For example, with reference to Figure 9, during steady-state operation, the primary switches 58, 60 block no more than the input voltage, V_{in} ; and the rectifiers block no more than twice the output voltage, $2 \cdot V_{out}$. As mentioned above, the switches and the rectifiers operate on balanced duty cycles (*i.e.*, the switching duty cycle of each element is comparable to that of its complementary element) and with a high power conversion duty cycle (*i.e.*, the sum of the duty cycles of the complementary switches is a large fraction of the total converter operating period). The switches and rectifiers are therefore efficiently utilized. Two short energy-recycling intervals introduce a relatively small amount of dead time in a converter period, which prevents realization of 100% power conversion duty cycle. The short energy-recycling intervals however improve conversion efficiency by reducing switching losses at high frequencies; reduce radiated and conducted noise by limiting slew rates of voltages and currents; and reduce stresses due to dV/dt and dI/dt on primary and secondary switching elements. Owing to the sinusoidal resonant current waveforms, the RMS current for the primary and secondary switching elements of a SAC is slightly greater than that of a corresponding "square-wave" DC-to-DC transformer topology resulting in slightly higher (I^2R) conduction losses. The RMS current of primary switching elements is further increased by a purposeful scaling of the magnitude of the magnetizing current to enable ZVS. However, this small compromise in increased RMS currents and conduction losses allows switching losses to be virtually eliminated, thereby providing for greater power

density, efficiency, and overall performance by enabling more efficient conversion at much higher switching frequencies.

In certain applications of a VTM, it is desirable to provide simple but fast responding protection against short circuits at the output of the VTM as well as protection against transient or continuous overloads. Fig. 25 shows a SAC 200, which is a modified version of the SAC 90 of Fig. 9. The SAC of Fig. 25 differs from that of Fig. 9 by the addition of diodes 190, 192 in parallel with each of the resonant capacitors 34, 32. The circuit in Fig. 25 may be controlled by an automatic switch controller 179 of the kind described above in connection with Fig. 22. Addition of the diodes in combination with the automatic switch controller and with appropriate circuit component values, as discussed below, provides the SAC of Fig. 25 with current limiting and short circuit protection features. The operation of the circuit of Fig. 25 will be explained in comparison to the operation of the circuit of Fig. 9.

As the load 120 on the circuit of Fig. 9 is increased, the resonant current I_L will increase, as will the peak-to-peak value of the voltage V_c . In the event of an overload, I_L and V_c will be limited solely by parasitic resistances in the circuit. In the circuit of Fig. 25, however, this will not be the case. Assume, for example, that the circuit is operating in steady-state at a load current, I_{out} , at which the peak-to-peak variation in V_c is slightly less than V_{in} . Under these circumstances the clamp diodes 190, 192 remain reverse biased and the circuit will operate essentially identically to the circuit of Fig. 9. If, however, the load is increased to a value that, in the absence of the diodes 190 and 192, would cause the peak-to-peak variation in V_c to be greater than V_{in} , then diodes 190 and 192 will clamp V_c preventing it from varying above V_{in} or below ground.

Fig. 26 shows an equivalent circuit of the converter of Fig. 25 assuming that diode 190 is clamping the voltage V_c to the input source voltage V_{in} . The voltages across the capacitors 32, 34 are clamped, circuit resonance is prevented and the current I_L flows into the input source, V_{in} , via diode 190. The effect of the clamp diode is shown in Figs. 27A and 27B. The current I_L rises and falls sinusoidally (Fig. 27A) and the voltage V_c rises until it equals V_{in} (Fig. 27B) between times t_s and t_{c1} . At time t_{c1} , the clamp diode conducts, resonance ceases and the current I_L begins to drop linearly because the resonant inductor 74 is clamped to a fixed voltage. Thus, between t_{c1} and t_z , V_c is clamped to V_{in} and I_L declines linearly toward zero. At time t_z , the automatic switch controller senses that I_L has reached zero and another cycle begins. Because, in this

clamped mode of operation, the current waveform is non-sinusoidal during a portion of each converter operating cycle, the operating frequency of the converter is lower than the characteristic resonant frequency.

In summary, the converter of Fig. 25 will operate as the SAC of Fig. 9 until the load reaches a current value at which the clamp diodes begin to conduct. Further increases in load will result in a decrease in operating frequency, under control of the automatic switch controller 179. Under short circuit conditions, the peak current in the primary will be limited approximately to $I_p = (V_{in}/\pi) * (N_p/N_s) * \sqrt{C_R/L_R}$. The output current may thus be limited by appropriately choosing the ratio of C_R to L_R .

One drawback of the current limiting scheme shown in Fig. 25 is that it requires that C_R and L_R to be set to specific values. This will not, in general, consistently result in the lowest-Q resonant circuit, which, as explained above, has many benefits, including improved converter operating efficiency and transient response time.

Current limiting to protect against transient overloads and abnormal conditions may, alternatively, be provided without the use of clamp diodes by sensing the current flowing in primary switching elements and limiting, with primary control circuitry, the power conversion duty cycle to limit these currents. Current sensing may be incorporated with reduced dissipation, *i.e.*, without inserting a resistance in series with the power train, by extracting the derivative of the resonant capacitor voltage, *i.e.*, by sensing the rate of change of the resonant capacitor voltage, which is directly proportional to the primary current, with a parallel network consisting of the series combination of a sensing capacitor and resistor. This technique for current limiting SACs is analogous to that which is taught in Vinciarelli, U.S. Patent 5,555,165, "Current Detection in Power Conversion," assigned to the same assignee as this application and incorporated by reference. The instantaneous current flow within a SAC, measured by sensing the rate of change of the resonant capacitor voltage, may also be used to control the output voltage, or current, of a SAC in normal operation. The output of the parallel network consisting of a series combination of a sensing capacitor and resistor may be an input to circuitry to control the power-conversion duty cycle of the SAC, either open-loop or as part of a closed voltage or current loop.

If in a SAC, such as the topology of Fig. 25, the resonant inductance, L_R , exhibits a high quality factor, Q , as defined above, and the output storage capacitors 56 are also high-Q devices,

oscillatory ringing and overshoot may develop in the output voltage owing to resonance between the storage capacitors and the resonant inductance. Addition of a damping circuit such as damping circuit 204 (shown in Fig. 28), comprising a damping resistor 208 and damping capacitor 206, may be used to reduce or eliminate the ringing.

5 A schematic of a preferred embodiment of a complete SAC converter 302, in which virtually all of the switching losses are eliminated, is shown in Figure 35. In the Figure, the SAC comprises a half-bridge, series resonant, converter 310 and input filtering, bias and converter control circuitry 312. The half-bridge, series resonant, converter 310 comprises: primary switches M1 and M2; resonant capacitors C_{res1} and C_{res2} ; transformer T1, comprising primary winding 314 (having an equivalent winding resistance R_{tp}) and secondary windings 316, 318 (having a total equivalent winding resistance R_{ts})(feedback winding 322 and bias voltage winding 324, included in control circuitry 312, are also part of transformer T1); resonant inductance L_{leak} 320 (which may comprise, in whole or in part, the primary-reflected leakage inductance of transformer T1); secondary synchronous rectifier switches M21 and M22; output filter capacitor C_{out} (having an equivalent series resistance represented by resistor R_{esr}); and a damping circuit comprising capacitor C_{damp} and resistor R_{damp} (which may comprise, in whole or in part, the equivalent series resistance of capacitor C_{damp}). Input filtering, bias and converter control circuitry 312 comprises: an input filter, comprising inductor L_{in} , equivalent damping resistance R_{lin} , and input capacitor C_{in} (having an equivalent series resistance represented by resistor R_{cin}); bias voltage circuitry comprising rectifier diodes D1 - D4 and bias filter capacitor C_{vcc} ; startup resistor R_{start} ; under-voltage lockout circuitry, comprising comparator U4, resistors R13, R15, R16 and R17 and voltage reference V_{ref} ; current limiting circuitry, comprising current limiting capacitor C_{lim} , diodes D5, D6 and D7, resistors R11, R12 and R14, capacitor C_{del} and comparator U3; automatic gate control circuitry comprising current sense capacitor C_{sen} , current sense resistor R_{sen} , lead inductor L_{lead} , lead resistor R_{lead} (which may comprise, in whole or in part, the equivalent series resistance of lead inductor L_{lead}), complementary switch control comparators U1 and U2, MOSFET switches M5 and M6, MOSFET control switches M3 and M4, and transformer T2 comprising primary gate control windings 326, 328 and secondary gate drive windings 330, 332, 334, 336; and a feedback network, comprising resistors R_{stop} and R_{min} and capacitor C_{min} .

When power is initially applied from input source V_{in} , capacitor C_{vcc} will charge via startup resistor R_{start} . When the voltage across C_{vcc} exceeds a pre-determined under-voltage lockout threshold, set by resistors R15 and R17 and reference voltage $V_{ref} = 5V$, the under-voltage lockout comparator U4 will turn switches M5 and M6 ON, enabling automatic circuit operation. Once automatic circuit operation begins, circuit operating bias voltage, V_{cc} (approximately equal to 15 volts), is generated by winding 324 on transformer T1 via the full wave rectifier comprising rectifiers D1 through D4. Throughout the discussion which follows, M5 and M6 are assumed to be ON.

In operation, the approximately square wave of voltage across the primary winding of transformer T1 (as discussed above with respect to Figures 9 and 10) is reflected into winding 322 in control circuitry 312. Lead inductor L_{lead} converts the square wave voltage at winding 322 into an approximately linear ramp of current, which flows in resistor R_{sen} , connected to the inputs to comparators U1 and U2. The current in capacitor C_{sen} also flows in R_{sen} . As explained in Vinciarelli, U.S. Patent 5,555,165, "Current Detection in Power Conversion," if the capacitive impedance of current sense capacitor C_{sen} (in this case, the capacitive impedance at the characteristic frequency of the converter 302) is large relative to the value of current sense resistor R_{sen} , as it is in the circuit of Fig. 35, the current in C_{sen} will be a scaled version of the current in resonant capacitor C_{res2} . Figure 36A shows the current in C_{sen} as a scaled version of the current in switch M1, including both a resonant and magnetizing current portion. The resonant portion of the current returns to zero at time t_1 . Figure 36B shows the current in L_{lead} for three different values of L_{lead} . Figure 36C shows the voltage across R_{sen} , which is proportional to the difference in the currents in Figures 36A and 36B. As shown in Figure 36C, a value of $L_{lead} = L_2$ results in the voltage across R_{sen} , V_2 , returning to zero at time t_1 , when the resonant portion of the current in switch M1 returns to zero; a relatively larger value of $L_{lead} = L_1$ results in the voltage across R_{sen} , V_1 , remaining at a positive value at time t_1 ; a relatively smaller value of $L_{lead} = L_3$ results in the voltage across R_{sen} , V_3 , being negative at time t_1 . As explained below, the preferred setting for L_{lead} is a value which is smaller than L_2 .

Comparators U1 and U2 have the same signals applied to their inputs, but with reversed polarities. Thus, neglecting rise and fall times, when the output of one comparator is high (at positive voltage), the output of the other is low (at ground). One input to comparators U1 and U2 is the voltage across R_{sen} (V_{rsen}) offset by a positive DC voltage, $V_{ref} = 5$ Volts. The other input to

comparators U1 and U2 is a signal, V_{fb} , fed back from the output of comparator U2 via a feedback network comprising resistors R_{stop} and R_{min} and capacitor C_{min} , and also offset by the positive DC voltage, $V_{ref} = 5\text{Volts}$. The offset in both signals enables use of a unipolar comparator to compare the two otherwise bipolar signals. As noted above, switches M5 and M6 are enabled during normal converter operation. Both M5 and M6 have a non-negligible channel resistance when ON and the switches are poled so that the anodes of the body diodes of M5 and M6 (not shown in the Figure) connect, respectively, to the gates of control switches M3 and M4. Figure 38 shows an equivalent circuit of switches M5 and M6, comprising a controllable ideal switch 354, a channel resistance represented by resistor R_c 350 and body diode represented by diode D_b 352. As shown in Figures 39A and 39 B, switches M5 and M6 can also be embodied as a circuit, comprising low resistance MOSFET 356 or bipolar switch 357 in series with a discrete resistor R_d 358, in parallel with a diode 359.

With reference to Figures 35 and 37, during the period $t = t_0$ to t_1 switch M1 is ON, switch M2 is OFF, the output of comparator U1 is high, the output of comparator U2 is low, switch M3 is ON and switch M4 is OFF. At time t_1 the signal V_{rsen} (Fig. 37A) declines below the signal V_{fb} (Fig. 37B), causing the output of comparator U1 to go low (Fig. 37C) and the output of comparator U2 to go high (Fig. 37D). The low-going output of U1 rapidly discharges the gate of M3 (Fig. 37E) through the body diode of switch M5, causing the gate voltage to pass through its threshold voltage at time t_2 , turning M3 OFF. The high-going output of U2 cannot turn switch M4 ON rapidly, however, because the channel resistance of switch M6 slows the charging of the gate of M4. Thus, the gate of M4 does not pass through its threshold voltage, and turn ON, until relatively much later, at time t_6 (Fig. 37F). With M3 and M4 both OFF during the period between t_2 and t_6 , the magnetizing inductance of transformer T2 resonates with the capacitive gates of primary switches M1 and M2 and synchronous rectifier switches M21 and M22, redistributing the energy among the gates and causing charging and discharging of the output parasitic capacitances of switches M3 and M4. The rise and fall of the voltages on the gates of switches M1 and M2 are shown in Figs. 37G and 37H, respectively. Because the threshold voltage (V_t) of each switch is positive, and because the ON or OFF state of each switch is determined by when its gate voltage passes through its threshold voltage, switch M1 turns OFF (at time t_3 , Fig. 37G) prior to the time at which switch M2 turns ON (at t_4 , Fig. 37H). The period between times t_3 and t_4 , when both switches M1 and M2 are OFF, is the energy-recycling interval, during which the

magnetizing current of transformer T1 charges and discharges the parasitic drain capacitances of M1, M2, as previously discussed. ZVS of switches M1 and M2 may be achieved during this interval by proper sizing of the magnetizing inductance of transformer T1. Commutation of the gate voltages and conductivity states of the synchronous rectifiers, M21 and M22, are similar to that of the gate voltages and conductivity states of switches M1 and M2, respectively, and are not shown in the Figure. Because switches M3 and M4 are both OFF between times t_2 and t_6 , ZVS of both M3 and M4 can also be achieved by proper sizing of the magnetizing inductance of transformer T2. At time t_5 , the drain of switch M4, having crossed zero is clamped by the body-drain diode of M4, thus clamping the voltage across winding 326 to essentially the bias voltage V_{cc} , thereby also clamping the winding voltages applied to the gates of switches M1, M2, M21 and M22. At time t_6 the gate of switch M4 passes through its threshold voltage and switch M4 turns ON at essentially zero voltage. At time t_4 switch M2 turns ON, leading to another power-transfer interval which ends one half-period later, at time $t_1+T/2$, where T is the converter operating period.

The timing relationships shown in Figure 37 for the SAC converter circuit of Fig. 35 depend on appropriate settings for the magnetizing inductances of transformers T1 and T2, the channel resistance of switches M5 and M6 (or the equivalent circuit resistance, as discussed above) and the value of L_{lead} . The magnetizing inductance of transformer T1 is selected to ensure that ZVS of switches M1 and M2 can be accomplished in a short time relative to the overall operating period of the converter, thereby effectively eliminating switching losses in M1 and M2 without unduly reducing the overall duty cycle of the converter. The magnetizing inductance of transformer T2 is selected to ensure that the commutation of the gate voltages of switches M1, M2, M21 and M22 (i.e., between times t_3 and t_4 in Figures 37G and 37H) occurs over a time period which is greater than or equal to the time required to achieve ZVS of the switches. If the magnetizing inductance of transformer T2 is made too small, the gate voltages will change too quickly and ZVS of M1, M2, M21 and M22 will not be completed. If the magnetizing inductance of transformer T2 is made too large, the gate voltages will change slowly and the losses in the switches will increase. The channel resistance of switches M5 and M6 (or the equivalent circuit resistance, as discussed above) is selected so that the time period t_2 through t_6 is longer than the time period between t_3 and t_4 , thereby ensuring ZVS of switches M3 and M4 and preventing early termination of the ZVS interval of switches M1, M2, M21 and M22.

Finally, the value of inductor L_{lead} is selected so that the times at which the resonant portion of the current in switches M1 and M2 returns to zero at the end of each power transfer interval corresponds closely to the point in time at which the switches turn OFF. Thus, in Fig. 37, the time at which it is desirable to have the resonant portion of the current in switch M1 return to zero corresponds to time t_3 , which is the time at which switch M1 turns OFF. Comparing the waveform for V_{rsen} in Fig. 37A to the waveforms in Fig. 36C, and with reference to the discussion of Fig. 36, it can be seen that the value of L_{lead} may be selected so that it is relatively lower than the value which would results in the voltage V_{rsen} returning to zero at the same time that the resonant portion of the current in switch M1 returns to zero. This accounts for the various delays in the circuit between the time that comparators U1 and U2 change state and the times that their associated primary switches cease conducting.

In Fig. 35, the impedance of capacitor C_{lim} is relatively small (at the characteristic frequency of the converter) compared to the impedance of the averaging circuit comprising diode D6, capacitor C_{del} and resistor R14. Thus, the current in C_{lim} is a scaled version of the primary resonant current and the average voltage across C_{del} and R14 is an averaged value of that current. Averaging is done over positive half-cycles; diode D5 carries the current in C_{lim} on negative half cycles. When the average value of resonant current exceeds a pre-determined threshold set by the values of resistors R11 and R12 and the value of V_{cc} (which is the approximate high-level voltage output of comparator U3), the output of comparator U3 goes low, disabling converter operation by disabling switches M5 and M6. The current limiter of Fig. 35 operates in a periodic mode: after the converter shuts down it will start up again and, if, after restarting, an over-current condition is still present, it will once again shut down. This process will repeat itself until the over-current condition is removed. Alternatively, a latch can be added to the circuit to keep the circuit shut down until input power is removed and reapplied.

When operated as described above, the gate driver circuitry Fig. 35, partially redrawn as low-loss, common source gate control topology 340 in Fig. 43, provides for ZVS of control switches M3 and M4 and of primary and synchronous rectifier switches M1, M2, M21 and M22 while also eliminating essentially all losses associated with the charging and discharging of gate capacitances of the primary and synchronous switches M1, M2, M21 and M22. By this means, the switching losses in the converter are essentially eliminated and the overall losses are reduced to the conduction losses in the channels of the switches. This virtual elimination of switching

losses enables high operating frequencies to be achieved at high conversion efficiency. In the low-loss, common source gate control topology of Fig. 43, the control input terminals (*i.e.*, the gate and source terminals) of the control switches M3, M4 share a common reference (*i.e.*, ground 342). Unlike prior art low-loss gate drivers using full or half-bridge topologies for control switches and suffering from the cost and performance limitations associated with driving “floating” switches, whose sources do not have a common DC reference, the control switches of Fig. 35 and of the low-loss, common source gate control topology of Fig. 43 can be controlled at high speed using simple, directly-coupled drive circuitry.

The low-loss, common source gate control topology of Fig. 43 is suitable for use in converters, such as SACs, in which switches are being controlled to operate at 50% duty cycle. Embodiments of low-loss, common source gate drive circuits adapted to operate over a range of duty cycles, including 50%, are shown in Figs. 44 and 45.

In Figure 44, switches M3 and M4 are complementary types (*e.g.*, switch M3 is an n-channel MOSFET and switch M4 is a p-channel MOSFET) and the diode 346 may be the body diode of switch M4 or it may be a discrete diode. Switch M4 and capacitor 344 form a “reset” circuit of the kind described in Vinciarelli, “Optimal Resetting of the Transformer's Core in Single-Ended Forward Converters,” U. S. Patent Re. 36,098, and in Vinciarelli et al, “Control of Stored Energy in Power Converter Transformers,” U. S. Patent 5,805,434, both assigned to the same assignee as this application and incorporated in their entirety by reference. If we assume that switch M3 is controlled by signal IN1 to be ON for a particular time interval at a particular duty cycle, then switch M4 is controlled by signal IN2 to be OFF during a continuous time interval which comprises the interval that switch M3 is ON plus a ZVS interval prior to switch M3 being turned ON and a ZVS interval following the time interval during which M3 was ON. As explained in the '098 and '434 patents, this provides for resetting of transformer T2 as the duty cycle varies over a range. The circuit of Fig. 44 is suitable for use in converter circuits in which a single primary switch may be operated at a duty cycle other than 50% or in converter circuits in which a pair of switches are operated in a mode in which the duty cycle of one switch may be other than 50% and the states of the pair of switches are complementary (*i.e.*, one is ON and the other OFF) throughout each converter operating cycle, except during the ZVS intervals. The source of switch M4 may alternatively be connected to a positive voltage, such as a “ V_{cc} voltage,” at an essentially DC level to ground for gate drive convenience. A limitation of the

low-loss, common source gate control topology of Fig. 44 is that gate voltages vary as a function of the duty cycles of the power switches and that switches that are ON for a greater fraction of the converter period are driven to a lower gate voltage.

In Figure 45 the low-loss, common source gate drive circuit 340 of Fig. 43 is modified by addition of a pair of inductive clamp circuits 345, 347, each comprising a switch 348, 349 and a diode 341, 343. Such a circuit is suitable for use in certain converters in which each switch is ON for a fraction of the converter operating period and in which the aggregate duty cycle of complementary switches is less than 100%. The switches 348, 349 are operated as taught in Prager et al, "Loss and Noise Reduction in Power Converters," U. S. Patent Application No. 09/834,750, assigned to the same assignee as this application and incorporated in its entirety by reference. In operation, signal IN1 controls switch M3 to be ON for a time interval (during which switch M2 is ON and switches M1, M4, 341 and 343 are OFF), after which switch M3 is turned OFF and switch 341 in clamp circuit 345 is turned ON by signal S1. This interrupts recycling of the magnetizing current of transformer T2 and clamps all the winding voltages near zero, holding all controlled switches (*e.g.*, switches M1, M2) OFF. When the time comes to turn switch M1 ON, switch 341 is first turned OFF, allowing for recycling of the magnetizing energy and commutation of the gate voltages on switches M1 and M2, after which switch M4 is controlled ON by signal IN2. Switch M4 remains ON for a time interval, after which switch M4 is turned OFF and switch 343 in clamp circuit 347 is turned ON by signal S2. The pair of inductive clamp circuits 345, 347 may be replaced by a single bi-directional inductive clamp switch, *e.g.*, connected between the drain of M3 and the drain of M4, subject to the availability of suitable bi-directional switching devices.

The inductive clamp circuit consisting of switches 345, 347 (or, alternatively, a single bi-directional switch) in Fig. 45 may be incorporated within the active clamp topology of Fig. 44 across winding 326 in order to provide a low-loss, common source gate drive topology for complementary switches having a different duty cycle and an aggregate duty cycle less than 100%.

Figure 47A shows a gate drive circuit, of the same type as the gate drive circuit comprising winding 330 in Figures 35, 43, 44 and 45, in which a transformer winding 331 is used to deliver a gate control voltage, V_{gs} , to a MOSFET switch 333. As shown in Figure 47B, the V_{gs} waveform for such a circuit swings between positive and negative values. Bipolar drive

in such a circuit is both unnecessary and undesirable: it is unnecessary because negative voltage is not needed to turn the MOSFET OFF (it is OFF when the gate voltage drops below the gate threshold voltage, V_T); it is undesirable because the current flow associated with the negative transitions results in superfluous losses in the circuit.

5 An improved gate drive circuit is shown in Figure 48A. In the Figure, two small MOSFET switches 335a, 335b are connected to each end of the winding 331. The winding is a secondary of a gate drive transformer T_D which is driven with a gate driver circuit of the kind described above with reference to Figures 35, 43, 44 and 45. Figures 48B and 48C show operating waveforms for a preferred embodiment of the circuit of Fig. 48A in which the gate

10 threshold voltage of the primary switch 333, V_{T333} , is greater than the gate threshold voltages of the small switches 335a, 335b, V_{T335A} and V_{T335B} . Prior to time t_1 , the primary switch 333 is ON and the voltage V_W is positive and equal to V_{ON} . Because V_{ON} is greater than the gate threshold voltages of MOSFET switches 333, 335A, both switches are ON. With switch 335A ON, the gate voltage on switch 335B is essentially zero and switch 335B is OFF. Under the steady state

15 conditions prior to time t_1 , the current in the winding may be assumed to be essentially zero and the voltage across switch 335A (V_{DS335A} , Fig. 48C) is also essentially zero. At time t_1 the drive to the gate drive transformer T_D is removed (e.g., switch M4 in the gate drive circuit of Fig. 43 is turned OFF, as described above) and the magnetizing current in the transformer commutates into the secondary winding 331, flowing as current I_W in the direction of the arrow in Fig. 48A. This

20 flow of current discharges the gate capacitance C_{gs} of primary switch 333 and the output capacitance C_{out} of small switch 335B, resulting in a decline in the gate voltage, V_{gs} (Fig. 48B) of switches 333 and 335A. The flow of current I_W also results in a voltage drop, V_{CH} , across switch 335A, as shown in Figure 48C. Since the voltage V_{CH} appears at the gate of switch 335B, it is important that channel resistance of switch 335A be selected to be low enough so that V_{CH} does

25 not exceed the gate threshold voltage of switch 335B, as this would result in switches 335A and 335B being ON at the same time and disrupt the operation of the circuit. At time t_2 the voltage V_{gs} declines below the gate threshold voltage of primary switch 333 (V_{T333} , Fig. 48B), causing switch 333 to turn OFF. At time t_3 , V_{gs} declines below the gate threshold voltage of small switch 335A (V_{T335A} , Fig. 48B), causing switch 335A to turn OFF. The voltage across switch 335A

30 (V_{DS335A} , Fig. 48C) begins to rise as the current I_W charges the output capacitance C_{out} of the switch. At time t_4 , the voltage across switch 335A increases above the gate threshold voltage of

switch 335B (V_{T335B} , Fig. 48C), turning switch 335B ON. The current I_W now flows in the channel resistance of switch 335B, resulting in a small negative voltage ($-V_B$, Fig. 48B), across the switch. The voltage across switch 335A (V_{DS335A} , Fig. 48C) continues to rise until time t_5 , at which time the voltage across switch 335A reaches its maximum value, V_{ON} . Some time after t_5 , complementary drive to the gate drive transformer T_D is restored (e.g., switch M3 in the gate drive circuit of Fig. 43 is turned ON, as described above). At time t_6 the complementary portion of the cycle begins by once again removing drive from the transformer T_D (e.g., switch M3 in the gate drive circuit of Fig. 43 is turned OFF, as described above). The waveforms for V_{gs} (Fig. 48B) between times t_6 and t_{10} are similar in form to the waveforms for V_{DS335A} (Fig. 48C) between times t_1 and t_5 and the waveforms for V_{DS335A} (Fig. 48C) between times t_6 and t_{10} are similar in form to the waveforms for V_{gs} (Fig. 48B) between times t_1 and t_5 . Thus, as illustrated in Figures 48B, the circuit of Figure 48A results in an essentially unipolar drive to the gate terminal of primary switch 333, eliminating the superfluous losses of the circuit of Figure 47A.

Where the gates of two MOSFET switches are driven in a complementary manner (i.e., the gate signal to one is high when the gate signal to the other is low) and the gate drive signals to the MOSFETs share a common return, as, for example, is the case for the secondary synchronous rectifier switches M21 and M22 of Fig. 35, the gate drive improvement of Fig. 47A may be implemented with further simplification, as shown in Figure 49. In the Figure, the two windings 334, 336 of Figure 35 are replaced with a single winding 334, thereby simplifying the construction of transformer T2. Switches 335a and 335b operate as described above for the circuit of Fig. 47A, resulting in an essentially unipolar gate drive for switches M21 and M22.

In the gate driver circuits of Figs. 48A and 49 the threshold voltages of switches 335A, 335B should be selected to be relatively low to minimize dissipation associated with discharge of the gate capacitance of the primary switch (e.g., switch 333, Fig. 48A; switches M21 and M22, Fig. 49). The threshold voltage of the primary switch must also be greater than or equal to the threshold voltages of switches 335A, 335B, to ensure, e.g. in Fig. 49, that both primary switches cannot be ON at the same time. One way to ensure that these conditions are met is to integrate the primary switches with the gate clamp switches, as illustrated in Fig. 53.

In Fig. 53 a semiconductor integrated power MOSFET 410 is schematically shown to comprise a power section 412, comprising a plurality of paralleled cells 412a - 412n, and a sense section 437 comprising a cell which is identical to cells in the power section 412. All of the cells

are designed so that their threshold voltage is relatively low. The source connections, 416a - 416n and 418, and gate connections, 420a - 420n and 421, of all cells in both the power and sense sections are connected together and terminated at source and gate connection terminals 427, 429. The drain connections 414a - 414n of all of the cells in the power section are connected together and terminated at drain connection terminal 431, whereas the drain connection 433 of the sense cell 437 is connected to a separate sense terminal 435. Since all of the cells are integrated onto the same semiconductor die, all will have essentially the same threshold voltage.

Fig. 54 shows a circuit of the kind shown in Fig. 49 that incorporates two integrated power MOSFETs 410a, 410b of the kind shown in Fig. 53. The power section 412a (412b) and sense section 437a (437b) of integrated MOSFET 410a (410b) replace switches M21 (M22) and 335B (335A) of Fig. 49 respectively as shown in Fig. 54. The drain terminals 435a, 435b of the sense sections of each device 410a, 410b are respectively connected, as clamps, to the gate terminals 429b, 429a of the other device. By connecting integrated power MOSFETs in this way, the threshold voltages of the clamp switches 437a, 437b and primary switches (formed by power cells 412a, 412b), which are presumed to be relatively low by design, are closely matched. As a result, if the gate voltage of a power cell reaches its threshold voltage value and turns the power cell ON, the clamp switch associated with that power cell will also turn ON, clamping the gate of the other power cell and ensuring that the other power cell is held OFF. More generally, the sense section of an integrated MOSFET may be used to clamp, hold OFF or turn OFF, other switches in other portions of the circuit when the power section of the integrated MOSFET is turned ON. This advantage of the integrated MOSFET is particularly useful in a variety of applications, including synchronous rectifier applications.

Another embodiment of the gate drive circuits of Figs. 48A and 49, using bipolar transistor switches 337A, 337B, is shown in Fig. 50. In the Figure, resistors 373A, 373B provide a path for turning bipolar switches 337A, 337B ON. Diodes 371A, 371B are connected across resistors 373A, 373B. As a bipolar switch is turned OFF, the voltage drop across its respective diode will subtract from the base-emitter voltage of the bipolar switch as charge is swept out of the base region of the bipolar switch. If the voltage drop of the diode is essentially equal to the base-emitter voltage of the bipolar switch, the voltages will cancel and the effective "threshold voltage" of the bipolar switch (i.e., the voltage equivalent to the voltages V_{T335A} and V_{T335B} in Figs. 48B and 48C) will be close to zero volts.

Diodes 375A and 375B (Figs. 48A, 49, 50), which may, in the case of MOSFET switches (e.g., switches 335A and 335B, Figs. 48 and 49) be the intrinsic body diode of the switch, provide a current path which enables startup of the circuit and which, in general, provides a path for current to flow in the poled direction of the diode when a switch is OFF.

5 Figures 40A and 40B, show, respectively, top and bottom perspective views 450a, 450b of an embodiment of the SAC of Figure 35, which includes another embodiment of a transformer of the kind shown in Figs. 32 and 33. The transformer 451 has two core element sets, each set comprising one of two core pieces 422a, 422b and one of two end pieces 424a, 424b. The end
10 pieces may be of a magnetic material or permeable medium different from that of the core pieces. The initial permeability of the end pieces may be relatively low and adapted to set the effective permeability the transformer to the low values required to optimize high frequency ZVS operation of the SAC. Thus, the initial permeability of the end pieces and of the core pieces may be selected from within a range of values, typically less than 10, which may be obtained from temperature stable, low permeability ferrites, or molded ferrite powder or other low-loss
15 high frequency magnetic media. The gaps between the end pieces 424a, 424b and their respective core pieces 422a, 422b may, therefore, be minimized to a mechanical clearance, as opposed to playing a first order role in setting the effective permeability of the core. Magnetic flux may be contained within the core and fringing may be minimized to reduce proximity losses in the windings.

20 Etches forming the windings (not shown) are part of multi-layer PCB 442. MOSFET switches 448, packaged in 5mm x 5mm square MLP packages, may be used for the primary switches and may be connected to the primary windings of the transformer via etches (not shown) on the PCB 442. The control circuitry described above with respect to Figures 35 through 39, with the exception of capacitors and transformer windings, is provided within an
25 integrated circuit 444. A drive transformer 457, corresponding to transformer T2 and comprising windings 326, 328, 330, 332, 334, 336 of Fig. 35, having a physical structure similar to that of transformer 451 and comprising core piece 423 and end piece 425 is used to drive the gates of main switches 448 and synchronous rectifier switches 453. Resonant capacitors 430, in conjunction with the leakage inductance of transformer 451, set the characteristic resonant
30 frequency of the converter. Input capacitors 456 provide a reservoir of energy and input filtering. The outputs of the synchronous rectifiers 453 connect to output capacitors 458, 460.

Windings for the transformers 451, 457 are not shown in Figure 40 but are of the kind described with respect to the transformer structure of Figures 32 and 33. As explained with respect to the example shown in Figs. 34A and 34B, the secondary windings associated with core sets 422a and 424a may be connected via synchronous rectifiers 453 to capacitors 458, and the secondary
5 windings associated with core sets 422b and 424b may be connected via synchronous rectifiers 455 to capacitors 460, to deliver two separate, isolated and filtered DC output voltages, V_1 and V_2 , at terminal pairs 462a, 462b and 464a, 464b, respectively. The two voltage outputs, V_1 and V_2 may be the same and the terminals 462, 464 may be connected in parallel to provide a single output with increased total power output; or the voltages may be the same or different and may
10 be used separately. The input voltage, V_{in} , may be delivered to the SAC 450 at input terminals 466a, 466b. A signal terminal 468 may be used to deliver a feedback signal to a PRM or power regulator front end, or it may be used for another purpose, *e.g.*, as an enable/disable input to control the outputs of the SAC. The overall dimensions of the SAC 450, including the over-molding epoxy (discussed above), may be $L = 1$ inch (25.4 mm), $W = 1$ inch (25.4 mm) and $H =$
15 0.2 inch (5mm).

The low-Q transformer structures used in preferred SAC embodiments are characterized by tightly coupled windings, which may be interleaved and exhibit relatively high primary-to-secondary parasitic capacitances. Figure 41 shows a portion of a SAC 380 of the kind illustrated in Figures 9 and 35, which includes two switches 390, 392 and a transformer 382 having
20 multiple primary windings 360, 361 and secondary windings 362 and 363 and which may be of the kind described with respect to Figures 32 and 33. Primary-to-secondary parasitic capacitances 383, 385 are shown to form a coupling path between the primary and secondary windings. Because the signals at the ends 387, 389 of the transformer primary windings are different, the signals coupled through capacitances 383, 385 will also be different and this will
25 result in a net coupling of unwanted switching signals into the output circuitry of the converter 380, resulting in the generation of undesirable common-mode noise across the converter. A way to minimize this problem is illustrated in Fig. 42. In the Figure, a converter 381 includes the same transformer structure 382 shown in Figure 41, but incorporates two additional switches 393, 394. The switches are driven in a complementary fashion *i.e.*, switches 390 and 394 are
30 driven ON and OFF in synchronism, as are switches 392, 393. The result is that the signals at transformer ends 387, 389 will be inverted versions of each other and the signals coupled

through primary-to-secondary parasitic capacitances will be of opposite polarity and thus essentially cancel each other. This common-mode noise cancellation mechanism relies on the soft-switching (i.e., ZVS) nature of the SAC converter of Fig. 42, the symmetry between the two halves of its power train circuit and its physical realization, as shown in Figs. 40a and 40b, to be effective at high frequency. However the two VTM outputs need not be paralleled and may operate at different voltages and loads as long as the outputs are tied symmetrically to a common ground. The technique illustrated in Figure 42 is easily adapted to the SAC embodiments of Figures 34 and 40 because the dog's bones transformer structures are naturally separable into the two halves shown in Figure 42. In both figures 41 and 42, the transformer may comprise two separate transformers as illustrated.

The common-mode noise cancellation mechanism for the SAC half-bridge topology described above is inherent to the SAC push-pull topology of Fig. 14 because of its inherent symmetry. The mechanism may also be applied to the SAC full-bridge topology of Fig. 12 by requiring a more complete symmetry of the full-bridge power train. This may be accomplished by the use of two resonant capacitors connected to the two ends of the primary winding or windings of the transformer as shown in Figs. 46A and 46B or, alternatively, by a single resonant capacitor connected to the opposite ends of two primary windings as shown in Fig. 46C. The incorporation of common-mode noise cancellation in SAC topologies for VTMs complements the inherently low levels of differential-mode noise stemming from the harmonic purity of Sine Amplitude Converters. The combination of low differential-mode and low common-mode noise performance of VTMs incorporating symmetric SAC topologies is particularly valuable in noise-sensitive power system applications, in addition to its general usefulness in reducing the filtering requirements necessary to achieve agency compliance with respect to conducted and radiated noise emissions.

If conventional transformer structures are used in the VTMs described above, there may be cases, for a particular factorized bus voltage, V_f , in which it may not be possible to design a VTM capable of delivering certain values of output voltage. For example, the output voltage of an ideal VTM which comprises a conventional magnetic transformer having a turns ratio N_s/N_p , is $V_{out} = T * V_f * N_s/N_p$, where T is a fixed constant relating to the VTM circuit topology (e.g., $T=1$ for a full bridge topology and $T=1/2$ for a half-bridge topology). The gain K of the VTM therefore includes the constant T . In such a VTM, N_s/N_p cannot be set to arbitrary values

because it is the ratio of two integer numbers (*i.e.*, the ratio of the integer number of turns on a secondary winding to the integer number of turns on a primary winding). One way to solve this problem is to use multiple factorized buses, as described above with respect to Figs. 7 and 8. If, for example, the primary of the transformer has 10 turns, then secondary turns of 1, 2, 3 and 4 will result in turns ratios, N_s/N_p , of, respectively, 0.1, 0.2, 0.3 and 0.4. If a factorized distribution bus provides a voltage, V_f , such that $T \cdot V_f$ is 50V, then output voltages of 5V, 10V, 15V and 20V can also be achieved using different turns ratios, but other output voltages, such as 3.3V or 12V, cannot. If, however, another factorized distribution bus is provided which delivers another factorized bus voltage, such that $T \cdot V_f$ is 40V, then the same set of turns ratios can deliver 4V, 8V, 12V and 16V, respectively. Likewise, another factorized bus at a voltage which provides $T \cdot V_f = 33V$ can produce VTM outputs of 3.3V, 6.6V, 9.9 V and 13.2 volts. In summary, by designing VTMs which are optimized to operate from different values of factorized bus voltages, V_f , and providing different transformation ratios, virtually any value of output voltage can be generated.

Another way to provide a range of VTM output voltages without using multiple factorized buses is to use transformer structures in which turns ratios are not limited to ratios of integers. Transformers of this type are described, *e.g.*, U.S. Patent No. 4,665,357, "Flat Matrix Transformer," incorporated by reference in its entirety. Generally, Faraday's law supports arbitrary transformer "turns ratios" based on the ratio of magnetic flux coupled to the primary and secondary windings of the transformer.

Multiple factorized distribution buses may also be used within the Factorized Power Architecture to provide very high levels of fault tolerance by eliminating single point failures associated with a single distribution bus. In particular, VTMs may be powered from multiple buses to support a critical load (*e.g.*, brakes in a car) or they may be automatically switched by selectively opening and closing switches (*e.g.*, low ON-resistance MOSFETs) in series with each VTM onto redundant factorized power buses, thus allowing power system flexibility at moderate costs by virtue of the inherent simplicity and low cost of VTMs.

A multiplicity of output voltages may be obtained from a multiplicity of VTMs or from multiple-output VTMs. For example, if, as shown in Fig. 21, the transformer 70 of the SAC of Fig. 9 is provided with two secondary windings 72a, 72b, the corresponding VTM will provide two output voltages, V_{out1} and V_{out2} , which will be related by the turns-ratios of their respective

windings. Thus, if each center-tapped secondary winding 72a, 72b has N_2 and N_3 turns, respectively, then the output voltage V_{out2} will be essentially equal to $V_{out1} * N_3 / N_2$. In multiple output VTMs care must be exercised to minimize and balance leakage inductance relating to secondaries of the transformer. Incremental, primary resonant inductance may be used to improve matching of resonant frequencies associated with multiple output SACs. The regulation and cross-regulation characteristics of multiple output VTMs incorporating SAC power trains will be superior to that of traditional power supplies with open-loop, “derived” auxiliary outputs because of the cancellation of reactive impedances which gives rise to an output resistance matrix, R_{out} , governing the load dependency associated with a multiplicity of outputs.

Power regulators (*see, e.g.*, Figs. 3, 6, 7, and 8) for use in FPA systems can be isolated and/or non-isolated and can use any of a variety of topologies, depending upon the input source (or sources) and other application requirements. As shown in Fig. 16, if the source is an AC utility source (*e.g.*, 110 or 220 VAC, 50/60 Hz), the power regulator 118 can comprise a combination of a utility source rectifier and conditioner 112 and an isolated, regulating DC-DC converter 114. In general, the power regulator 118 will generate a controlled, DC output voltage, V_f , which is relatively low (*e.g.*, 48V, 24V) compared to the peak value of the AC source and which is galvanically isolated from the AC source for safety reasons. The AC source 116 voltage is delivered to the input of the rectifier and conditioner 112, which produces a unipolar output voltage, V_{dc} . The voltage V_{dc} is delivered to the input of the isolated DC-DC converter 114, which generates the controlled voltage, V_f , for delivery to inputs of VTMs. Where harmonic attenuation or power factor correction is not required, the rectifier and conditioner 112 can comprise a full-wave or half-wave rectifier and storage capacitors for smoothing the rectified AC source voltage. Where harmonic attenuation or power factor correction is desired, the rectifier and conditioner 112 can comprise a non-isolated boost switching converter controlled by a power factor correcting controller or it can comprise a passive harmonic attenuator of the kind described in U.S. Patent Application No. 09/944,737, “Passive Control of Harmonic Current Drawn from an AC Input by Rectification Circuitry,” assigned to the same assignee as this application and incorporated by reference in its entirety. Alternative approaches to interfacing with AC utility lines include use of a single stage, isolated, power-factor-correcting front end. *See e.g.*, U.S. Patent No. 6,069,801, “Power Factor Correction in Switching Power Conversion,” assigned to the same assignee as this application and incorporated by reference in its entirety.

If the input source is a relatively high voltage DC source, the power regulator can comprise the same topological features, including isolation for safety reasons, as those described above for an AC utility source, except that there will be no requirement for rectification, power factor correction and/or harmonic attenuation. As shown in Fig. 17, if the DC input source 124 is at a relatively low voltage (*e.g.*, nominally 48 VDC or below), a non-isolated switching regulator 122 can be used to generate the controlled voltage V_f for delivery to the inputs of VTMs. The non-isolated switching regulator can be a buck, boost, or buck-boost converter depending on the range of variation of the voltage, V_s , delivered by the DC input source and the desired value of V_f .

With reference to Fig. 3A, the voltage, V_{in} , at the input to a VTM 44 in an FPA system 36 will generally be slightly different from the voltage, V_f , delivered to the factorized distribution bus 40 by the power regulator 38, owing, for example, to voltage drops in the distribution bus. Variations in the voltage, V_{in} , delivered to the input of a VTM will produce a proportional variation at the output, V_{out} . Where losses in the distribution system are small, their effect on the output voltages of VTMs will also be small. However, in certain cases it may be desirable to actively regulate the output voltage of a VTM.

One way to actively regulate the output voltage of a VTM is illustrated in Figure 18. In the Figure, the output voltage, V_{out} , of a VTM 136 is regulated by use of a feedback controller 126 which compares the VTM output voltage, V_{out} , to a reference signal V_{ref} (not shown), indicative of the desired value of V_{out} , and uses an error between V_{out} and V_{ref} to generate a control signal, V_{ctl} , delivered to a control input 128 of the power regulator 126, as a means of reducing or eliminating the error. In the feedback architecture of Fig. 18, V_{ctl} is used by the power regulator 126 to control the magnitude of V_f to maintain the output voltage of the VTM at the desired value. The feedback controller may be realized as a stand-alone device, as shown in Fig. 18, or it may be incorporated either within the Power Regulator or within the VTM.

Another method to actively regulate the output voltage of a VTM is illustrated in Figure 19. In the Figure, the output voltage of a VTM 136 is regulated by use of a feedback controller 126 which compares the VTM output voltage, V_{out} , to a reference signal (not shown) indicative of the desired value of V_{out} , and uses an error between V_{out} and V_{ref} to generate a control signal, V_{ctl} , delivered to a control input 128 of the PRM 191, as a means of reducing or eliminating the

error. The feedback loop and signal paths may be contained within the subassembly where the PRM 191 and VTM 136 are located (remotely from the front end 39).

In certain applications, the VTM may be located remotely from the point-of-load and the voltage at the point-of-load, V_L , may be lower than the voltage, V_{out} , at the output of the VTM.

One method to actively regulate the voltage at the point-of-load is shown in Fig. 20. In the Figure, sensing leads 193, 194 deliver the voltage V_L at the point-of-load to a feedback controller 126. The feedback controller (which may be locally powered by the voltage V_L) monitors the value of V_L , compares it with an internal reference signal V_{ref} , and generates a control signal, V_{ctl} , delivered to the control input of a remote power regulator (*e.g.* 38 in Fig. 3A) or a remote PRM (*e.g.* 43 in Fig. 3B).

In certain applications, the power requirements of a load may exceed the power capability of a single VTM and an array of VTMs may need to be paralleled to support the load.

Furthermore, in applications that call for fault tolerant back up of point-of-load converters, arrays of paralleled converters may be used to share the load among the converters. An example of a

power sharing array of VTMs 136A, 136B, 136C having their inputs and outputs connected in parallel to feed a load 41 is shown in Fig. 31. As discussed above, current sharing among paralleled VTMs is a function of the relative output resistance, R_{out} , of each VTM. As also

described above, current sharing accuracy may be greater with SACs than with non-resonant VTMs. Accuracy of point-of-load voltage may be increased using a feedback architecture. A

PRM 191 is shown in Fig. 31 supplying a controlled voltage V_f to the VTMs. The voltage at the point-of-load may be actively regulated using the architecture shown in Figs. 18, 19, or 20. In

Fig. 31, sensing leads 193, 194 deliver the voltage V_L at the point-of-load to a feedback

controller 126 (similar to Fig. 20). The feedback controller (which may be locally powered by the voltage V_L) monitors the value of V_L , compares it with an internal reference signal V_{ref} , and

generates a control signal, V_{ctl} , delivered to the control input of the PRM 191 (or a remote power regulator, *e.g.* 38 in Fig. 3A, or a remote PRM, *e.g.* 43 in Fig. 3B). The presence of such a

feedback loop complements the simple, scalable power-sharing attributes of an array of

paralleled VTMs with high bandwidth, high DC gain point-of-load regulation and without the active circuitry and wiring complexities and attendant single point system failure mechanisms,

stability issues, limited performance and high cost, or any of many other potential downfalls and limitations, of arrays of DC-DC converters.

To enable point of load regulation, DC-DC converters, may be flexibly deployed to complement VTMs within the Factorized Power Architecture or conventionally within a Distributed Power Architecture. In Figure 55A, a DC-DC converter 480 comprises a non-isolated power converter 482 which accepts a DC input voltage V_{in} and delivers a regulated voltage, V_{reg} , to the input of a DC-to-DC transformer 484. The DC-to-DC transformer delivers an output voltage V_{out} to a load (not shown). In Figure 55B, the DC-DC converter 485 comprises the non-isolated power converter 482 and DC-to-DC transformer 484 arrangement of Fig. 55A along with a feedback control circuit 490 which controls the output voltage, V_{out} , by delivering a feedback signal, V_{sig} , to the non-isolated power converter. The control circuit may also deliver control signals 492 to the DC-to-DC transformer, as described below in connection with Figs. 29A-29C.

The non-isolated power converter in Figures 55A and 55B may be a buck converter, a boost converter, or a buck-boost converter. A preferred buck-boost DC-DC conversion topology suitable for use as the non-isolated power converter 482, described in Vinciarelli, "Buck-Boost DC-DC Switching Power Conversion," U.S. Patent Application No. 10/214,859, filed August 8, 2002, assigned to the same assignee as this application and incorporated here by reference, allows for heretofore unprecedented efficiency and power density levels.

A Sine Amplitude Converter may be used to provide the DC-to-DC Transformer function in the DC-DC converters of Figs 55A and 55B. As further illustrated in Figs. 29A-29C, a SAC may be combined with a non-isolated power converter such as a buck pre-regulator, as shown in Fig. 29A, a boost pre-regulator, as shown in Fig. 29B, or a buck-boost pre-regulator, as shown in Fig. 29C. Alternatively, a bootstrap voltage regulator, as shown in Fig. 30, may be used to provide incremental power processing for conditioning the input voltage to the SAC in order to regulate the SAC output voltage.

Turning to Fig. 29A, a sine amplitude converter 201 incorporates an automatic switch controller (not shown). The voltage transformation ratio, or voltage gain, of the SAC, V_{out}/V_{reg} , is K. The output voltage of the SAC 201 is monitored by control circuit 121, which contains a voltage reference (not shown) and an error amplifier (not shown). The control circuit 121, which may be also interfaced to the SAC by one or more control lines 111, directs the opening and closing of the buck power switch 141. The switching frequency of switch 141 may, or may not, be locked to the resonant frequency of the SAC. The duty cycle of switch 141 (and rectifier 143)

is varied to regulate the voltage, V_{reg} , fed to the input of the SAC and, indirectly, the voltage, V_{out} , delivered by the SAC to the external load. The example of buck topology shown is only indicative of this general class of switching regulators. The buck pre-regulator may, for example, incorporate circuitry (not shown) to achieve efficient, high frequency ZVS operation of the buck switch 141, such as the active clamp topology and timing architecture disclosed in U.S. Patent Application Serial no. 09/834,750, entitled "Loss and Noise Reduction in Power Converters," filed April 13, 2001, assigned to the same assignee as the present application, and incorporated herein by reference. Assuming that the input voltage, V_{in} , is greater than V_{min} , and that the buck pre-regulator is capable of duty cycles up to 100%, the DC-DC converter of Fig. 29a is able to regulate the output voltage, V_{out} , from zero up to a value approximately equal to $K * V_{min}$.

Turning to Fig. 29B, a sine amplitude converter 201 provides a voltage transformation ratio approximately equal to K. The output of the SAC is monitored by control circuit 121. The control circuit 121, which may be also interfaced to the SAC 201 by control lines 111, coordinates the opening and closing of the boost power switch 147. The switching frequency of switch 147 may, or may not, be locked to the resonant frequency of the SAC. The duty cycle of switch 147 is varied to regulate the voltage, V_{reg} , fed to the input of the SAC and, indirectly, the voltage, V_{out} , delivered by the SAC to the external load. The example of boost pre-regulator topology shown is only indicative of this general class of switching regulators. The pre-regulator may incorporate circuitry (not shown) to achieve efficient, high frequency ZVS operation of the boost switch, such as the active clamp topology and timing architecture disclosed in "Loss and Noise Reduction in Power Converters," *ibid*. Assuming that the input voltage, V_{in} , is less than V_{max} and that the boost pre-regulator is capable of duty cycles down to 0%, the DC-DC converter of Fig. 29B is able to regulate the output voltage, V_{out} , down to a value approximately equal to $K * V_{max}$.

Turning to Fig. 29C, a sine amplitude converter 201 provides a voltage transformation ratio approximately equal to K. The output of the SAC is monitored by control circuit 121. The control circuit 121, which may be also interfaced to the SAC 201 by control lines 111, coordinates the opening and closing of one or more switches (e.g., switches 477, 479, 481, 483) in the buck-boost converter 487. The switching frequency of switches 477 - 483 may, or may not, be locked to the resonant frequency of the SAC. The duty cycle of switches 477 - 483 is

varied to regulate the voltage, V_{reg} , fed to the input of the SAC and, indirectly, the voltage, V_{out} , delivered by the SAC to the external load. The example of the buck-boost pre-regulator topology shown is only indicative of this general class of switching regulators. The pre-regulator may incorporate circuitry (not shown) to achieve efficient, high frequency ZVS operation of the buck-boost switches, such as the topologies and timing architecture described in Vinciarelli, “Buck-Boost DC-DC Switching Power Conversion”, *ibid*.

Cascading a SAC with buck or boost class pre-regulators, as in Figs. 29A and 29B, limits the efficiency and power density of the DC-DC converter by the combination of heat and volume of its constituent power stages, each of which is sequentially engaged in processing all of the power converted from source to load. Serial power processing within a DC-DC converter incorporating a SAC, or other DC-to-DC transformer stages, can be avoided, as shown in Fig. 30, by a parallel, “bootstrap” power processing architecture. The bootstrap architecture is characterized by generating within the SAC (or DC-to-DC transformer stage) 203 a floating, auxiliary output, V_{aux} , which is converted by an auxiliary regulator 232 to a boost voltage source, V_{boost} , stacked in series between the input, V_{in} , to the DC-DC converter 310 and the input to the SAC. The boost voltage source is set to the level required to control the voltage, V_{reg} , fed to the input of the SAC and, indirectly, the voltage, V_{out} , delivered by the SAC to the external load at the output of the DC-DC converter 310. The voltage transformation ratio of the auxiliary output of the SAC, $K_{aux} = V_{aux}/V_{in}$, may be chosen in concert with the minimum gain, K_{amin} , and maximum gain, K_{amax} , of the auxiliary regulator 232 to minimize overall power processing and maximize overall DC-DC converter efficiency. Based on these respective gain values and an input voltage range, V_{min} to V_{max} , the voltage, V_{out} , at the output of the DC-DC converter, may be regulated within the following range:

$$[K * V_{max} / (1 - K_{aux} * K_{amin})] < V_{out} < [K * V_{min} / (1 - K_{aux} * K_{amax})].$$

If the input voltage, V_{in} , is supplied by the controlled factorized bus of a Factorized Power Architecture, then $V_{max} = V_{min} = V_{in} = V_f$ and the extent of bootstrap power processing may be limited to the minimum necessary to effect a combination of DC-DC converter requirements, which may include closed-loop compensation of the output voltage and output voltage trimming. Assuming, for example, an output voltage trim range of 10% and a line/load compensation requirement of 3 %, the incremental power processing to perform the required complement of DC-DC converter functions could be kept to 25% or less, depending on operating

conditions. Assuming that this relatively small, incremental power processing is realized efficiently and with high density, the overall efficiency and density of a bootstrap regulated DC-DC converter for use in a FPA system could approach the figures of merit of VTMs.

Preferred embodiments of the bootstrap regulated DC-DC converter topology of Fig. 30 combine the SAC topology of Fig. 9 with an auxiliary synchronous buck switching regulator or with a synchronous boost switching regulator or with a synchronous buck-boost switching regulator. Another preferred embodiment provides the regulation function by means of a synchronous magnetic amplifier.

Figure 51 shows a simplified schematic of the SAC of Figure 35 modified to comprise feedback regulation circuitry 406 which modulates the resistance of primary switch MOSFETs M1 and M2 as a means of compensating for typically small variations in V_{out} that might otherwise be caused, *e.g.*, by voltage drops due to load current flowing in the output impedance of the SAC or by variations resulting from small changes in V_{in} .

Without the feedback regulation circuitry 406, the DC output voltage of the SAC is approximately equal to: $V_{out} = (N_s / N_p) * V_p - R_o * I_o$, where, with reference to Fig. 51, V_p is the absolute value of voltage across the primary winding of transformer T1 when switch M1 or M2 is ON; N_s and N_p are, respectively, the number of turns on the secondary and primary windings of transformer T1; R_o is the equivalent output resistance of the SAC; and I_o is the output current delivered by the SAC to the load 339. In the half-bridge topology of Fig. 51, V_p is approximately equal to $V_{in}/2$.

In operation, an error amplifier 400 compares the SAC output voltage, V_{out} , to a reference voltage 401 having a value V_{ref} indicative of the desired DC value of V_{out} . The output of the error amplifier, V_{er} , is delivered to a voltage regulator 402 as a means of varying the voltage, V_{cc} , delivered by the voltage regulator to gate driver circuitry 409 (which is of the kind shown in Fig. 35, comprising switches M3, M4 and transformer T2). The magnitude of the voltages V_{g1} and V_{g2} , delivered to the gate control terminals of primary switches M1 and M2, vary in proportion to V_{cc} .

Varying V_{g1} and V_{g2} causes the ON resistance of the switches M1 and M2 to vary. For a given load current, I_o , this variation in ON resistance will result in a variation in the voltage drop across the MOSFET which will be reflected as a variation in both V_p and V_{out} . Thus, if V_{out} drops below its desired set point, the regulation circuitry 406 will act to increase V_{g1} and V_{g2} , thereby

causing the ON resistances of M1 and M2 to decrease. The decrease in ON resistance causes V_p and V_{out} to increase, thereby counteracting the change in V_{out} . Because this means of regulation is dissipative, it is primarily useful for controlling variations of output voltage over a relatively narrow band.

5 The technique described above, in which the equivalent output resistance of a power converter is varied by varying the ON resistance of primary switches in the power converter, can also be used to perform “soft-start” (in which the magnitudes of the converter input current and output voltage are controlled to rise smoothly when power is applied to the converter) and output current limiting. This is of particular importance in SACs because the currents which flow at
10 startup (when the output filter capacitance is being charged from zero volts to the final value of the converter output voltage) or under short-circuit conditions, can be very large owing to the very low output impedance of the SAC.

 Soft-start may be achieved by controlling the rate of rise of the peak voltage applied to the gate control inputs of the primary switches. For example, in the converter of Figure 51, soft-
15 start may be achieved by incorporating circuitry (not shown) in the V_{cc} regulator 402 for controlling the rate at which V_{cc} rises when input voltage, V_{in} , is applied to the converter. This will result in a controlled rise in the amplitudes of V_{g1} and V_{g2} . As the peak values of V_{g1} and V_{g2} pass through a range near the threshold voltage of the primary switches M1 and M2, the ON resistance of the switches, and the equivalent output resistance of the converter, will vary
20 smoothly from a relatively high value to a relatively low value. This will reduce the peak currents that flow as the converter output filter capacitors (part of filter in 339) charge to their final values.

 Current limiting may be accomplished by measuring the output current of the converter and controlling the gate voltages of the main switches in order to keep the current at or below a
25 predetermined level. One way to measure the output current is to place a resistive element in series with the load. This, however, adds additional loss. Alternatively, a current transformer may be placed in series with the secondary or primary winding of power transformer T1. Another way to measure the output current is to sense the leakage flux in the power converter transformer (e.g., transformer T1, Fig. 51) as described in Vinciarelli et al, U. S. Patent
30 5,659,460, “Switch Control in Quantized Power Converters” (incorporated in its entirety by reference)(the “’460 patent”). As explained in the ‘460 patent, a sense loop may be placed

adjacent to the core of a power converter transformer (e.g., a loop formed by a conductive trace on a printed circuit board adjacent the transformer may be used) so that the leakage flux emanating from the transformer core couples the sense loop. The sense voltage induced in the sense loop by the leakage flux will be proportional to the rate-of-change of current in the transformer. Since the rate-of-change of transformer current and the converter output current will vary in proportion to each other, the sense voltage in the sense loop may be used to indicate the magnitude of the output current. Current limiting may therefore be accomplished as shown in Figure 52.

In Figure 52, leakage flux 417 from transformer T1 couples sense loop 415, generating a sense voltage, V_{sense} , as described above and in the '460 patent. Error amplifier 411 compares the magnitude of V_{sense} to a reference 413, V_{ref2} , which is indicative of the value to which the output current is to be limited. The output of the error amplifier, I_{er} , is delivered to the V_{cc} regulator 402 to control the value of V_{cc} as a means of controlling the ON resistance of the primary switches M1, M2, and thus the output current, I_{outs} of the power converter, in a manner similar to that described for the voltage controller of Fig. 51.

The technique of controlling V_{cc} as a means of controlling ON resistance may be used for both output voltage control and current limiting, as indicated in Fig. 52 by the use of a summing junction 419 for combining the voltage error signal, V_{er} , and the current error signal, I_{er} . To avoid excessive power dissipation due to continuous operation of M1 and M2 in a linear mode, a time out function may be used to latch down the converter in response to a persistent abnormal condition.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.